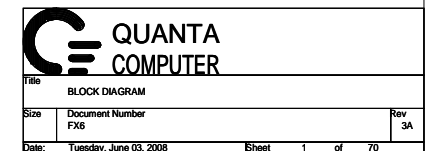


POWER



INDEX

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2	Index/Power States and USB/PCI/PCIe map
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12-15	SB700 page
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18-23	Blank
24	LCD/CRT HYBRID
25	Clock Generator
26	LCD Conn.
27	CRT Conn
28	HDMI
29	FAN /THERMAL
30	SATA (HDD&CD_ROM)
31-32	Audio CODEC(92HD73)/Phone Jack
33-34	LOM /Switch
35-36	PC CARD/1394
37	EXPRESS
38	USB
39	Mini Card
40	WWAN
41	Flash ROM, RTC
42	ITE8512
43	TP/KB/CIR/BT
44	Switch,Keyboard & LED
45	System Reset Circuit
46	RUN POWER
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48	DCIN,Batt
49	1.8V_SUS,0.9VTT
50	1.5V_RUN AND 1.1V_RUN
51	+VCC_NB
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54	+1.2V_ALW_SUS
55	Blank
56	Power Rail for system
57	Power Sequence Diagram
58	SMBUS BLOCK
59	Stitch caps and Screw hole.

USB PORT#

DESTINATION

SB700	0	Left side USB.
	1	Left side USB.
	2	IO board
	3	IO board
	4	WLAN
	5	WWAN
	6	WPAN
	7	EXPRESS
	10	Biometric
	11	Camera

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CardBus	AD17	REQ#1/GNT#1	IRQ_SERIRQ IRQD

PCI EXPRESS	DESTINATION
Lane 1	WLAN
Lane 2	WPAN
Lane 3	LOM
Lane 4	EXPRESS CARD
Lane 5	WWAN

PM TABLE

State	power plane	+15V_ALW +5V_ALW +3.3V_ALW	+5V_SUS +3.3V_SUS +1.8V_SUS +0.9V_DDR_VTT +1.2V_ALW_SUS	+5V_RUN +3.3V_RUN +2.5V_RUN +1.8V_RUN +1.2V_RUN +1.5V_RUN +VCC_CORE +NB_VCORE
S0		ON	ON	ON
S3		ON	ON	OFF
S5 S4/AC		ON	OFF	OFF
S5 S4 on Battery		OFF	OFF	OFF

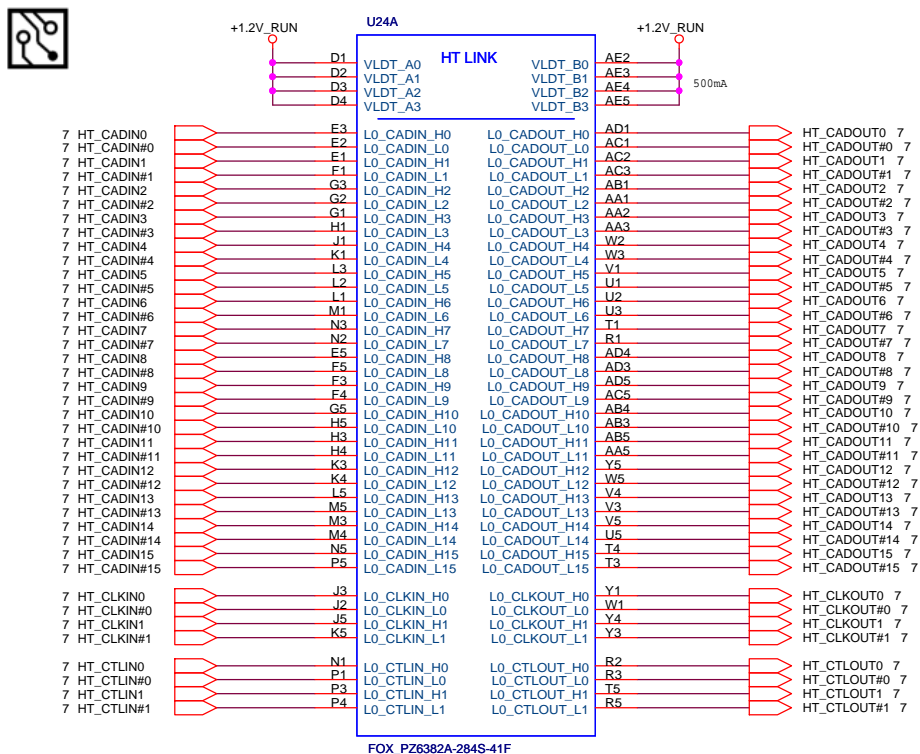
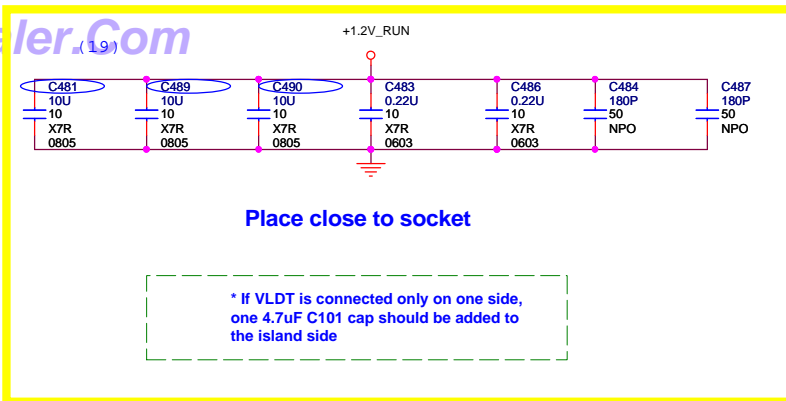
POWER STATES

State	Signal	SLP S3#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON)		HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF)		LOW	LOW	ON	OFF	OFF	OFF



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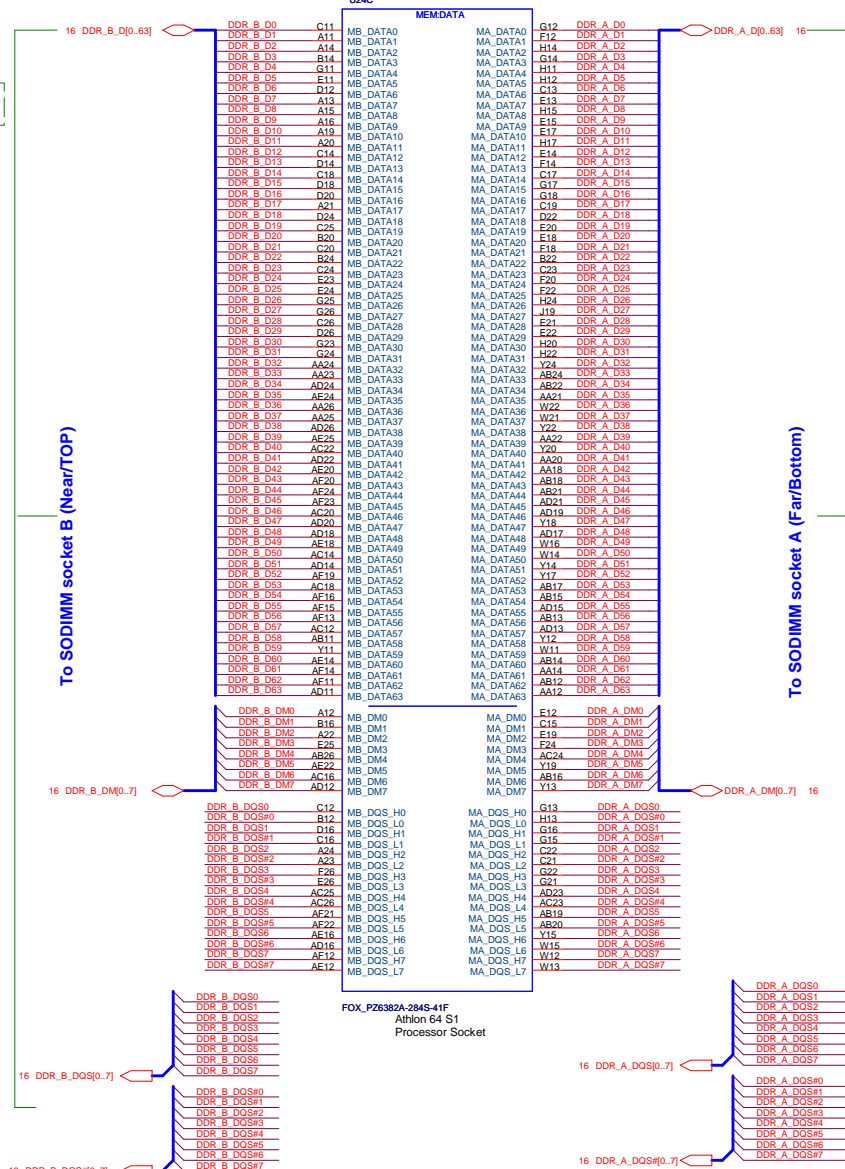


FOX_PZ6382A-284S-41F

Title: S1G2 HT I/F		
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1124C

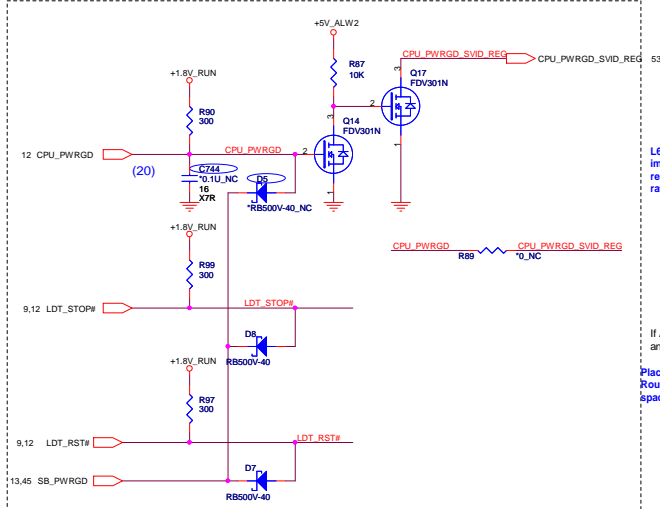
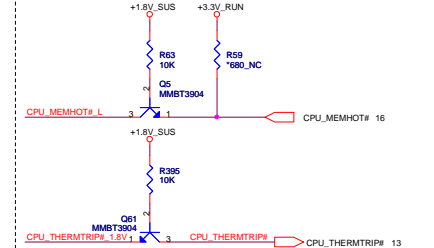
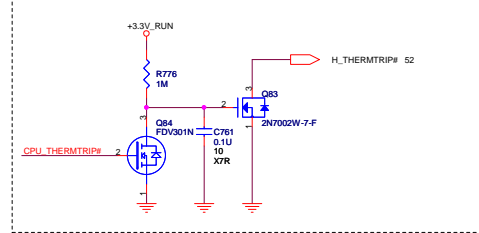
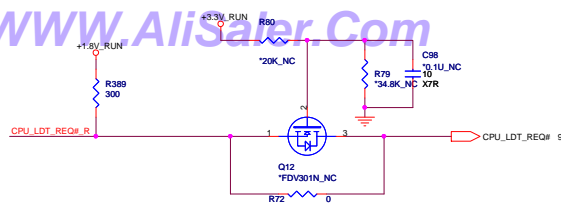
Place Capacitors for +0.9V_CPU_M_VREF_SUS < 1" from the RS780. +0.9V_CPU_M_VREF_SUS trace length < 6", trace width > 15mils and 20mils spacing from any adjacent signals in X, Y, Z directions.



PLACE CLOSE TO CPU
sensing point for
op-amp feedback
routed near CPU

PLACE CLOSE TO CPU
sensing point for
op-amp feedback
routed near CPU

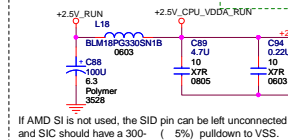
Date: Wednesday, June 25, 2008



L65 ferrite bead with an approximate impedance of 33 Ω maximum DC resistance of 0.025 ohm, and a current rating of at least 3000mA.

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG. This trace should be kept at least 20 mils away from all other signals.

+2.5V_CPU_VDDA_RUN



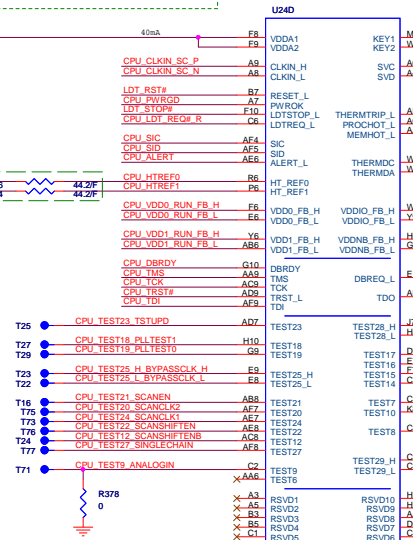
If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300- (5%) pull-down to VSS.

Place R78 and R77 < 1.5". Route CPU_HTRF1/0 with 5mils trace width and 10mils spacing from other signals in X, Y, Z directions

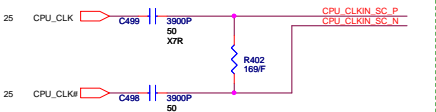
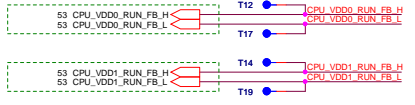
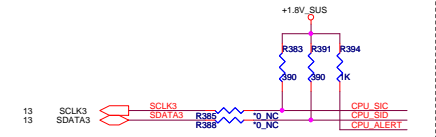


2-Bit Boot VID Codes

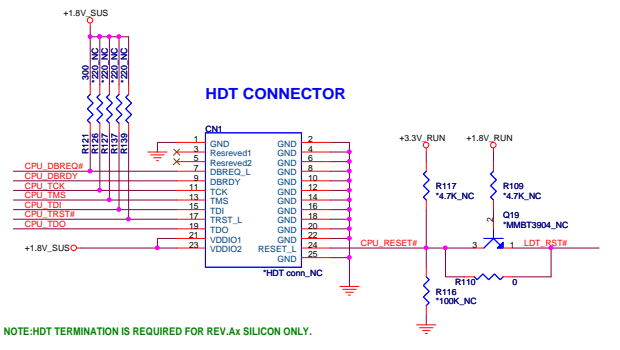
SVC	SVD	Voltage Output (CPU Power)
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V



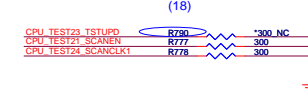
FOX_P26382A-284S-41F



1. KEEP TRACE TO RESISTOR LESS THAN 600MILS FROM CPU PIN AND TRACE TO AC CAPS LESS THAN 1.2".
2. CPUCLK and CPUCLK# mismatch < 35 mils.

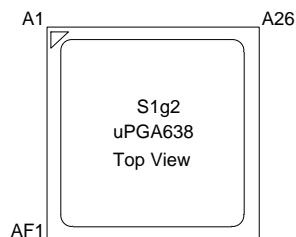
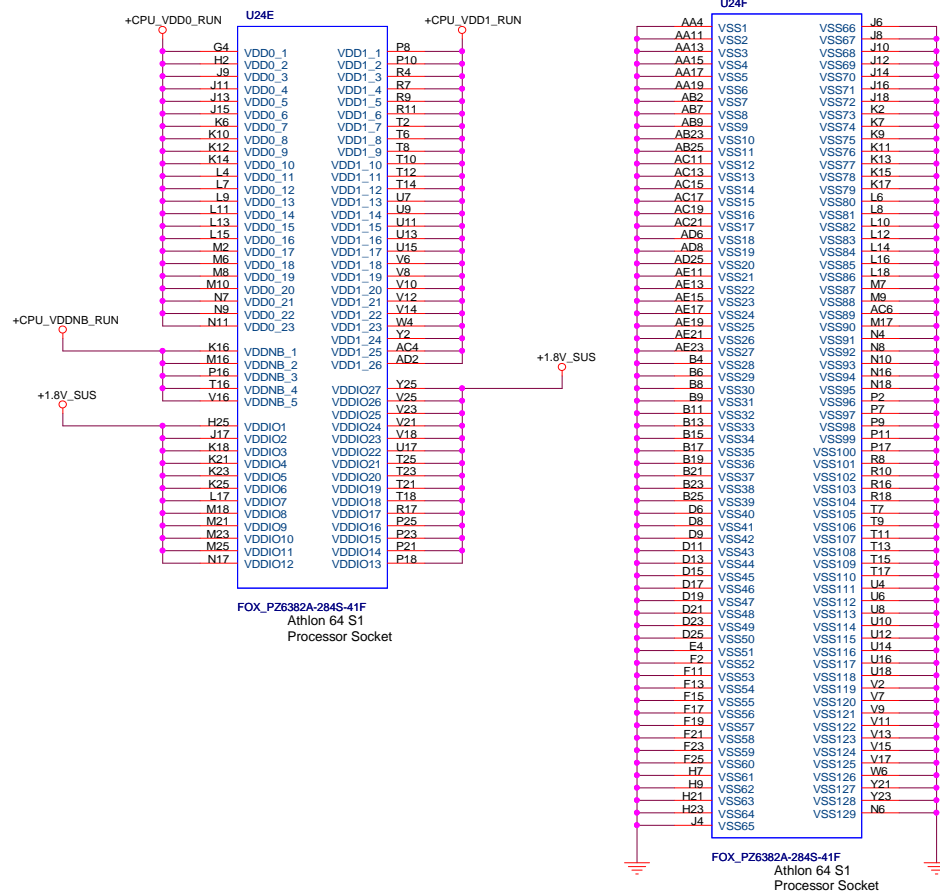


NOTE:HDT TERMINATION IS REQUIRED FOR REV.Ax SILICON ONLY.

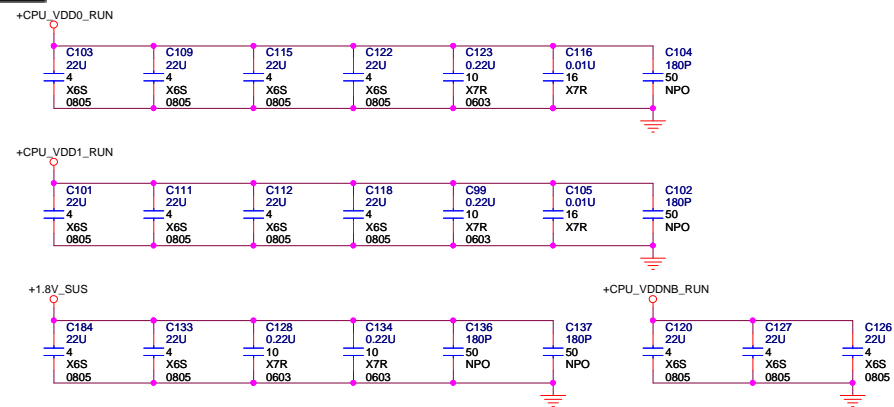


If no use which Net need pull-up or down

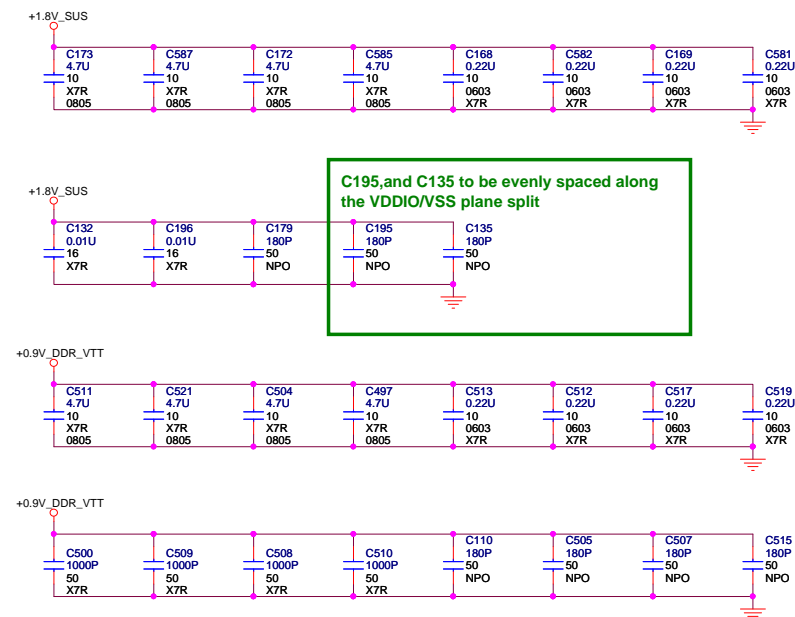
PROCESSOR POWER AND GROUND



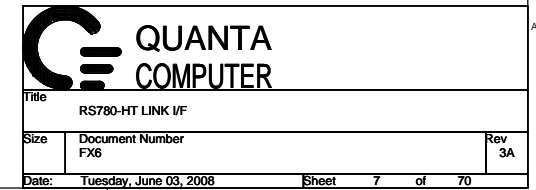
BOTTOMSIDE DECOUPLING

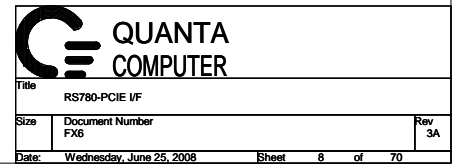


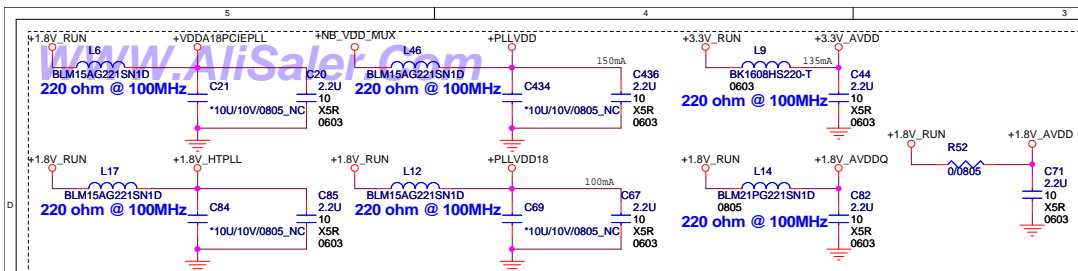
DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



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S1G2 PWR & GND		
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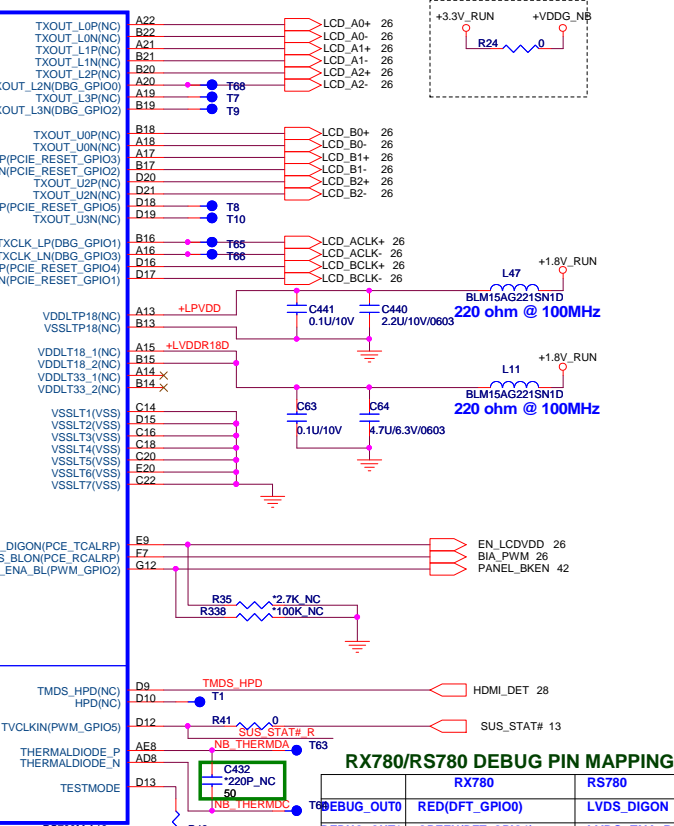
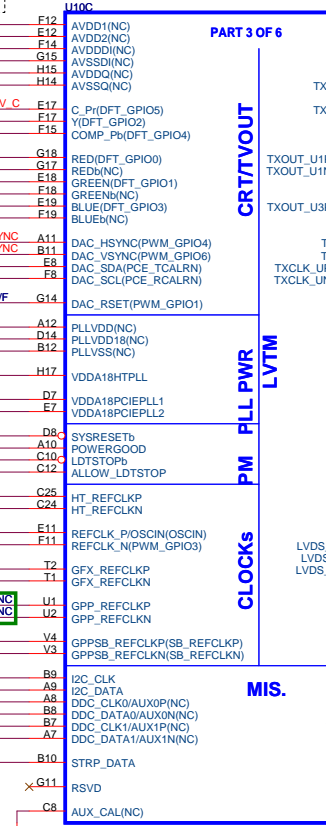
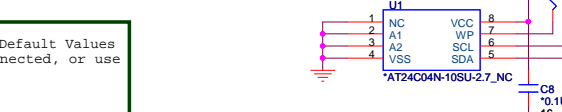
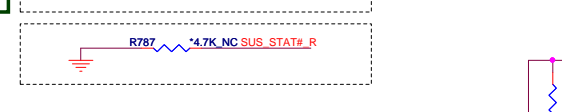
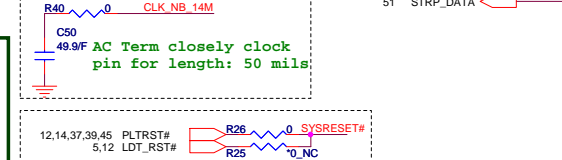
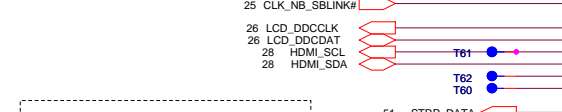
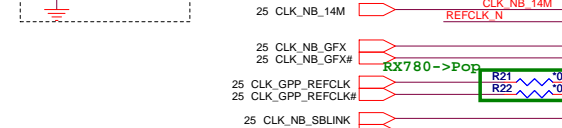
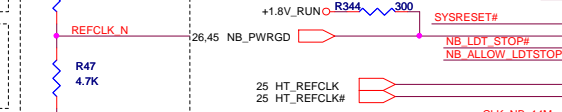
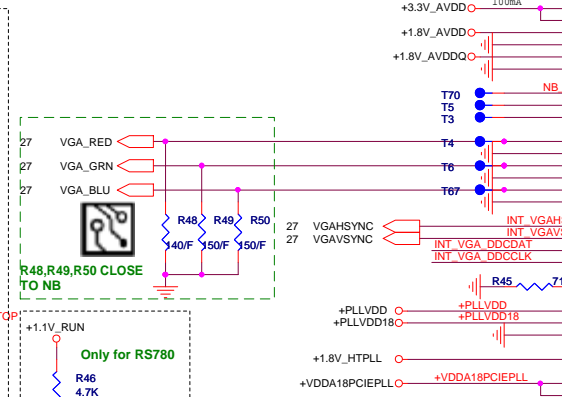
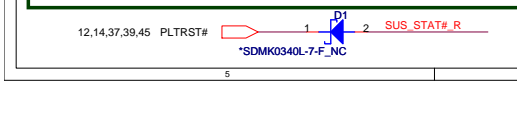
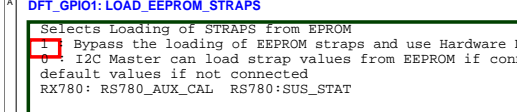
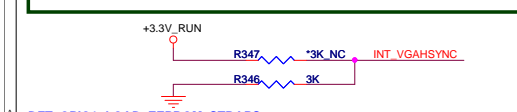
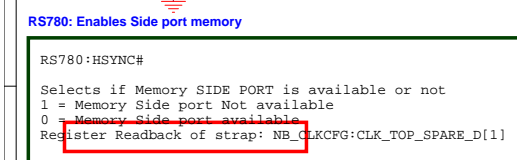
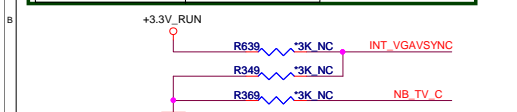
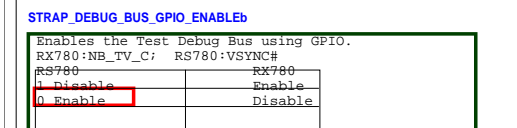
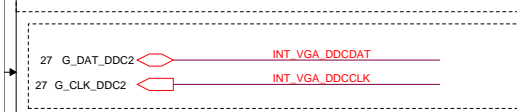
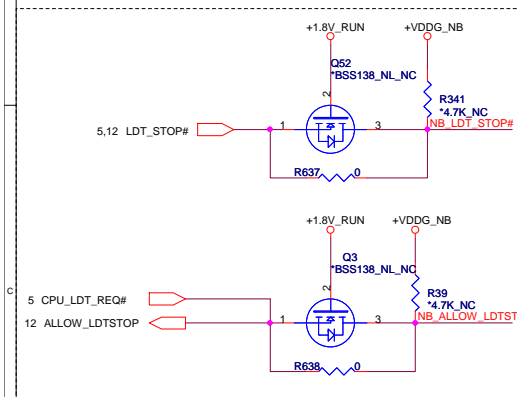
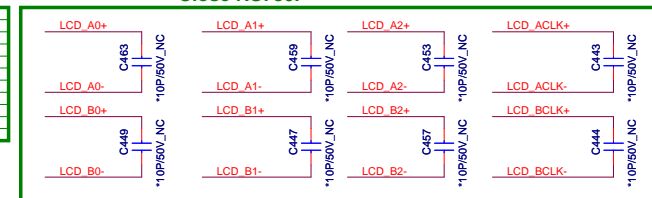




RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780
AVDD1	NC	+3.3V
AVDD2	NC	+1.8V
AVDD3	NC	+1.8V
AVDD4	NC	+1.8V
AVDD5	NC	+1.8V
AVDD6	NC	+1.8V
AVDD7	NC	+1.8V
AVDD8	NC	+1.8V
AVDD9	NC	+1.8V
AVDD10	NC	+1.8V
AVDD11	NC	+1.8V
AVDD12	NC	+1.8V
AVDD13	NC	+1.8V
AVDD14	NC	+1.8V
AVDD15	NC	+1.8V
AVDD16	NC	+1.8V
AVDD17	NC	+1.8V
AVDD18	NC	+1.8V
AVDD19	NC	+1.8V
AVDD20	NC	+1.8V
AVDD21	NC	+1.8V
AVDD22	NC	+1.8V
AVDD23	NC	+1.8V
AVDD24	NC	+1.8V
AVDD25	NC	+1.8V
AVDD26	NC	+1.8V
AVDD27	NC	+1.8V
AVDD28	NC	+1.8V
AVDD29	NC	+1.8V
AVDD30	NC	+1.8V
AVDD31	NC	+1.8V
AVDD32	NC	+1.8V
AVDD33	NC	+1.8V
AVDD34	NC	+1.8V
AVDD35	NC	+1.8V
AVDD36	NC	+1.8V
AVDD37	NC	+1.8V
AVDD38	NC	+1.8V
AVDD39	NC	+1.8V
AVDD40	NC	+1.8V
AVDD41	NC	+1.8V
AVDD42	NC	+1.8V
AVDD43	NC	+1.8V
AVDD44	NC	+1.8V
AVDD45	NC	+1.8V
AVDD46	NC	+1.8V
AVDD47	NC	+1.8V
AVDD48	NC	+1.8V
AVDD49	NC	+1.8V
AVDD50	NC	+1.8V
AVDD51	NC	+1.8V
AVDD52	NC	+1.8V
AVDD53	NC	+1.8V
AVDD54	NC	+1.8V
AVDD55	NC	+1.8V
AVDD56	NC	+1.8V
AVDD57	NC	+1.8V
AVDD58	NC	+1.8V
AVDD59	NC	+1.8V
AVDD60	NC	+1.8V
AVDD61	NC	+1.8V
AVDD62	NC	+1.8V
AVDD63	NC	+1.8V
AVDD64	NC	+1.8V
AVDD65	NC	+1.8V
AVDD66	NC	+1.8V
AVDD67	NC	+1.8V
AVDD68	NC	+1.8V
AVDD69	NC	+1.8V
AVDD70	NC	+1.8V
AVDD71	NC	+1.8V
AVDD72	NC	+1.8V
AVDD73	NC	+1.8V
AVDD74	NC	+1.8V
AVDD75	NC	+1.8V
AVDD76	NC	+1.8V
AVDD77	NC	+1.8V
AVDD78	NC	+1.8V
AVDD79	NC	+1.8V
AVDD80	NC	+1.8V
AVDD81	NC	+1.8V
AVDD82	NC	+1.8V
AVDD83	NC	+1.8V
AVDD84	NC	+1.8V
AVDD85	NC	+1.8V
AVDD86	NC	+1.8V
AVDD87	NC	+1.8V
AVDD88	NC	+1.8V
AVDD89	NC	+1.8V
AVDD90	NC	+1.8V
AVDD91	NC	+1.8V
AVDD92	NC	+1.8V
AVDD93	NC	+1.8V
AVDD94	NC	+1.8V
AVDD95	NC	+1.8V
AVDD96	NC	+1.8V
AVDD97	NC	+1.8V
AVDD98	NC	+1.8V
AVDD99	NC	+1.8V
AVDD100	NC	+1.8V

Close RS780.



RX780/RS780 DEBUG PIN MAPPING

	RX780	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLOK
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	AUX_CAL
	COMB_Pb(DFT_GPIO4)	X
	C_Pr(DFT_GPIO5)	X

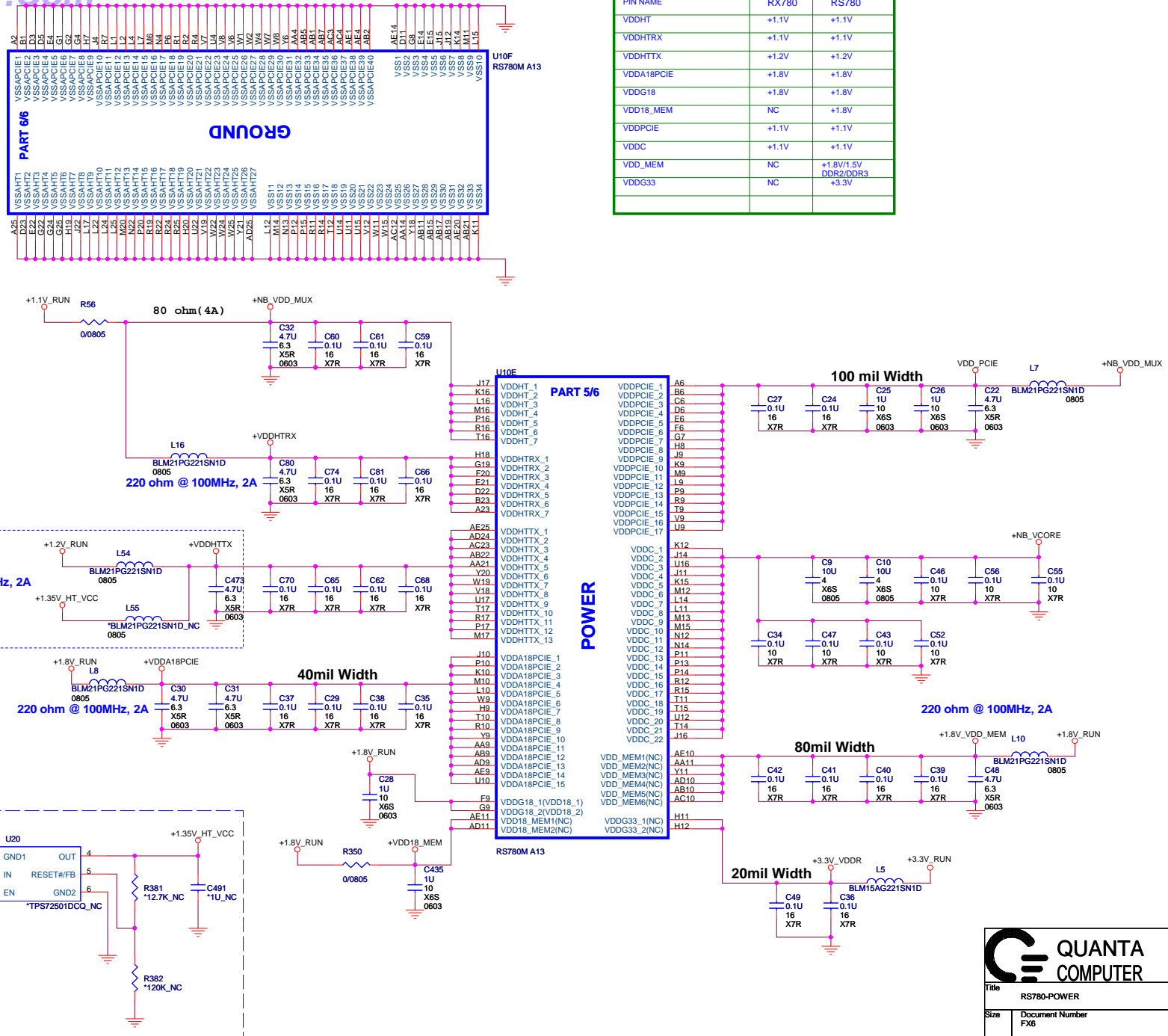


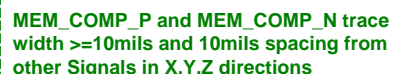
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NOTE: ACCESS TO STRAP_DATA AND I2C_CLK PINS IS MANDATORY.

PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V
VDDHTTX	+1.2V	+1.2V
VDDA18PCIE	+1.8V	+1.8V
VDDG18	+1.8V	+1.8V
VDD18_MEM	NC	+1.8V
VDDPCIE	+1.1V	+1.1V
VDDC	+1.1V	+1.1V
VDD_MEM	NC	+1.8V/1.5V DDR2/DDR3
VDDG33	NC	+3.3V





ALL external components connected to SPMEM signals must be removed for RX780.

0.9V_MEM_VTT

MEM_A8
MEM_A0

RP24

4

3

1

*4P2R-47

NC

C467

0.1U/10V

+1.8V_MEM_VDDQ

MEM_A2
MEM_A6

RP26

4

3

1

*4P2R-47

NC

C433

0.1U/10V

+1.8V_MEM_VDDQ

MEM_A7
MEM_A9

RP27

4

3

1

*4P2R-47

NC

C431

0.1U/10V

MEM_A11
MEM_A4

RP25

4

3

1

*4P2R-47

NC

C469

0.1U/10V

+1.8V_MEM_VDDQ

MEM_BA0
MEM_BA2

RP30

4

3

1

*4P2R-47

NC

C442

0.1U/10V

MEM_A5
MEM_A10

RP32

4

3

1

*4P2R-47

NC

C468

0.1U/10V

+1.8V_MEM_VDDQ

MEM_BA1
MEM_A1

RP31

4

3

1

*4P2R-47

NC

C448

0.1U/10V

MEM_A12
MEM_A3

RP28

4

3

1

*4P2R-47

NC

C454

0.1U/10V

+1.8V_MEM_VDDQ

MEM_CS#
MEM_ODT

RP22

4

3

1

*4P2R-47

NC

C437

0.1U/10V

MEM_CAS#
MEM_RAS#

RP23

4

3

1

*4P2R-47

NC

C470

0.1U/10V

+1.8V_MEM_VDDQ

MEM_CKE

RP29

4

3

1

*4P2R-47

NC

C466

*0.1U/10V_NC

MEM_WE#

RP29

4

3

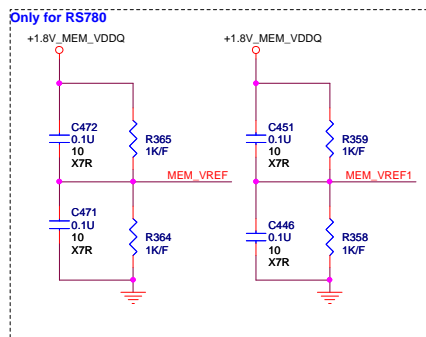
1

*4P2R-47

NC

C430

0.1U/10V



Place R580,R578
< 100mils from pins E27,E28,E29

 C310 AND C312 CLOSE TO 11600 P24

Place the translation circuit for CPU_PWRGD close to the SB700 to minimize stubbs when the circuit is No Stuff.

PLACE THESE COMPONENTS CLOSE TO SB700, AND
USE GROUND GUARD FOR 32K_X1 AND 32K_X2
ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM.

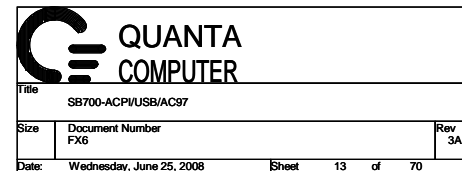
Option to "Disable" clkrun.
Pulling it down will
keep the clocks running.

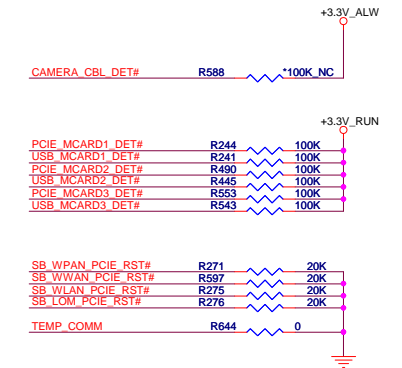
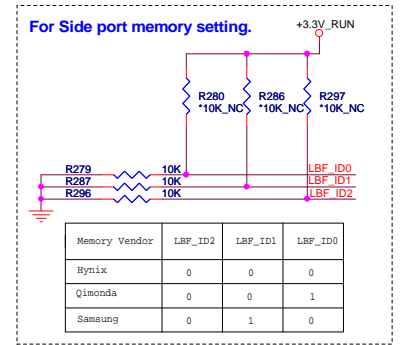
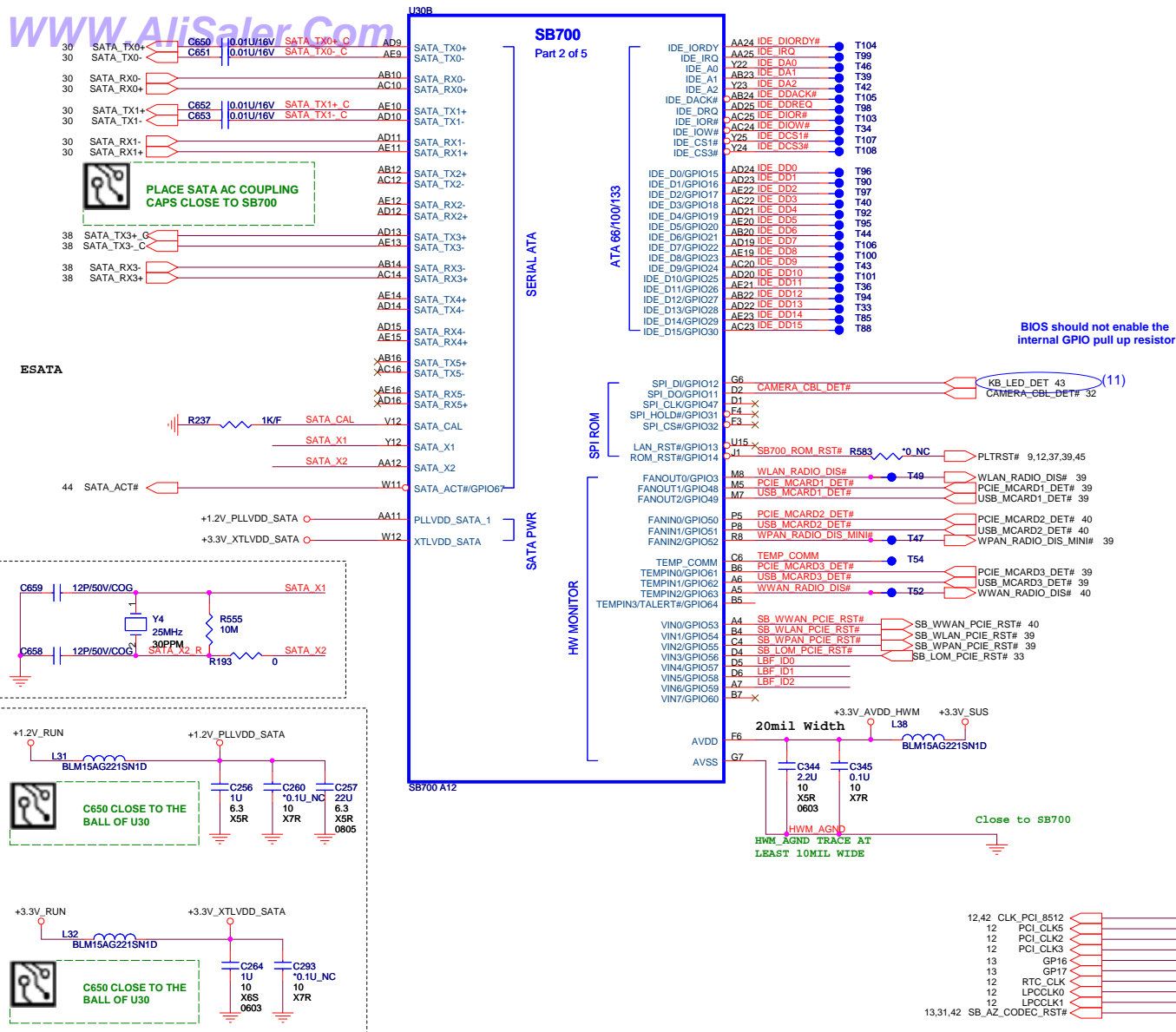
CMOS Clear
(Top or easy access place)



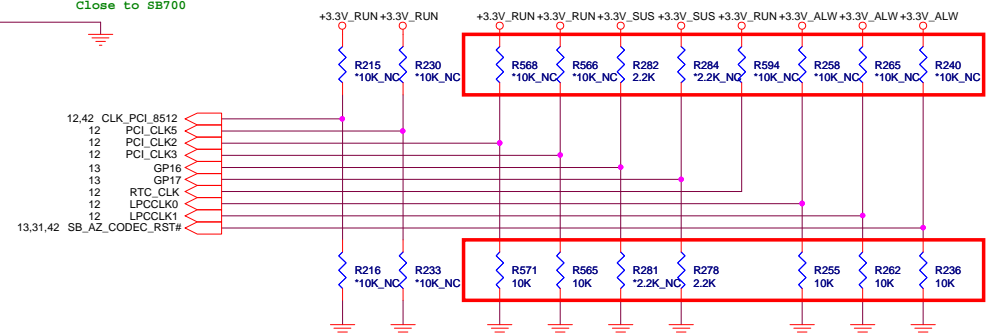
QUANTA
COMPUTER

Title			
SB700-PCIe/PCI/LPC			
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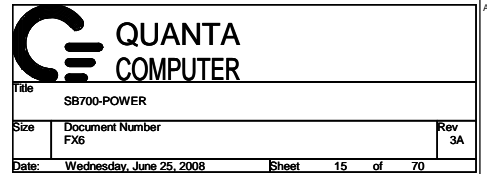


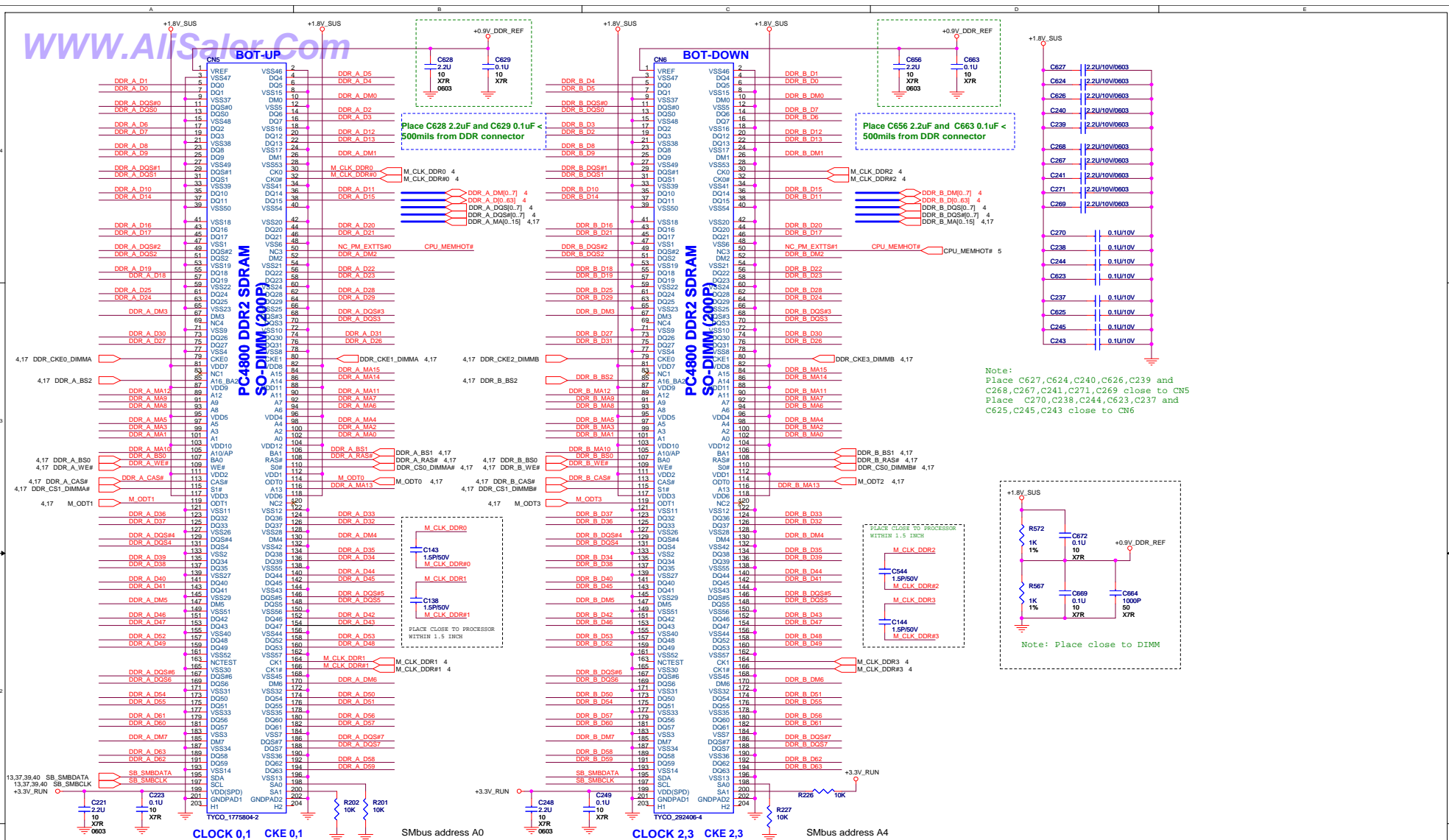


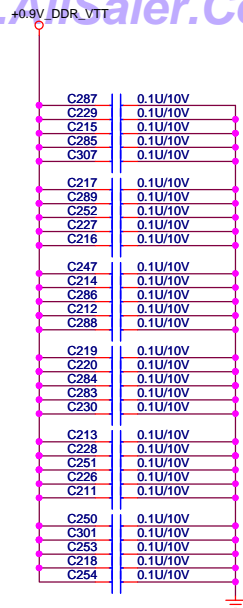
REQUIRED STRAPS



	PCI_CLK2	PCI_CLK3	LPC_CLK0	LPC_CLK1	RTC_CLK	SB_AZ_CODECS_RST#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM	DEFAULT

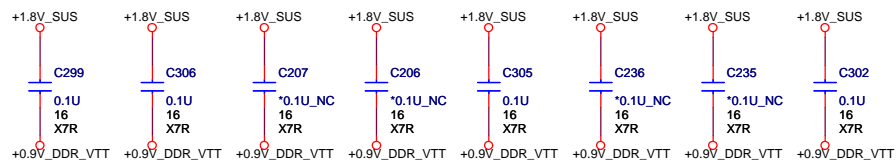




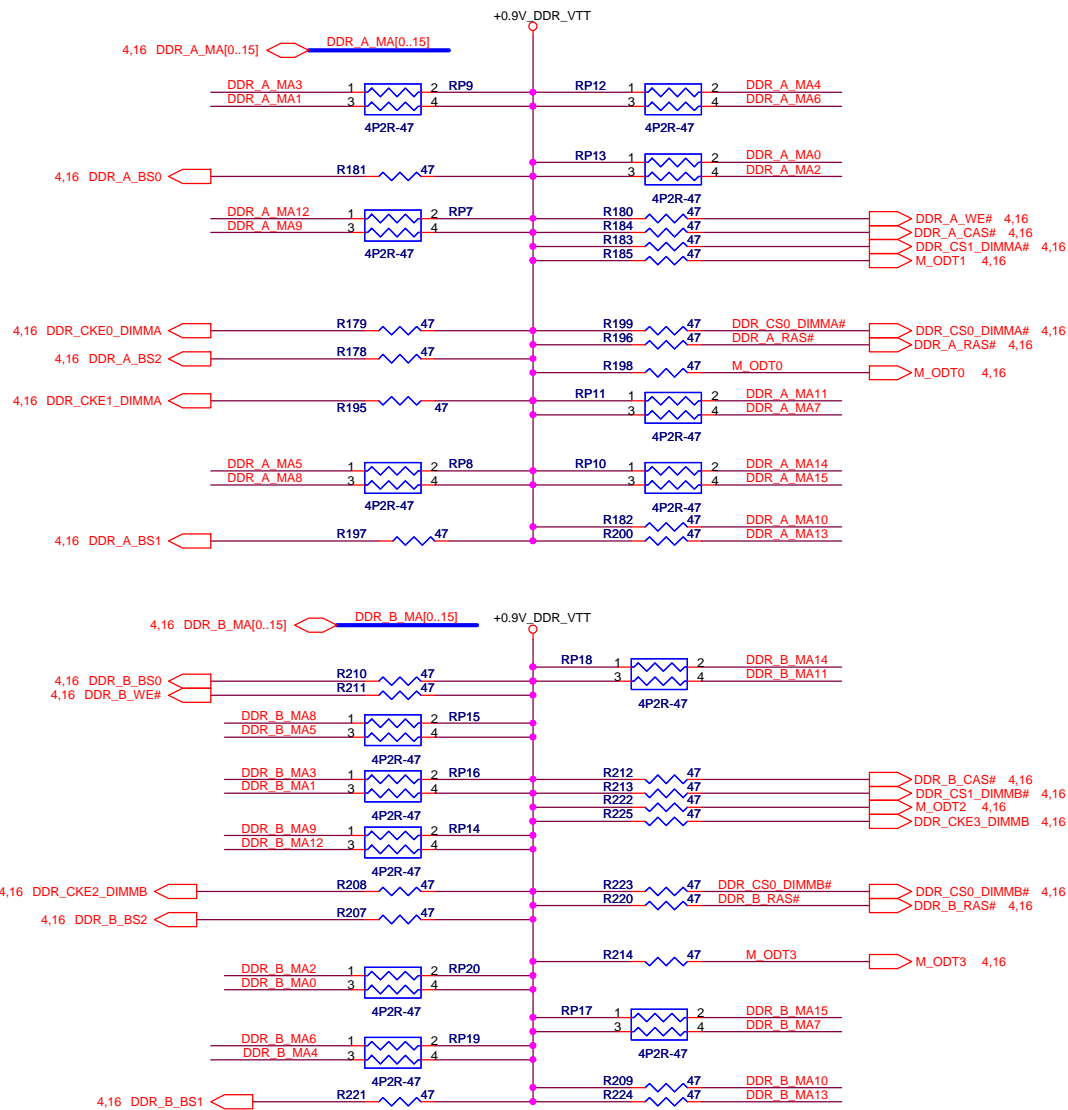
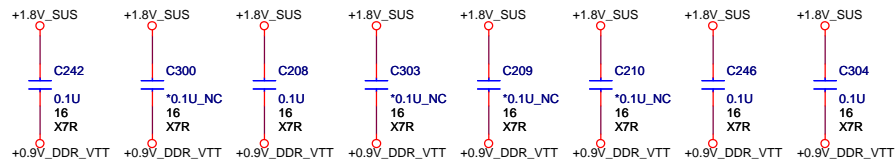


Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT

Note: Reserve stitching function for CN5.



Note: Reserve stitching function for CN6.



Title: DDRII TERMINATION		
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Custom	FX6		3A
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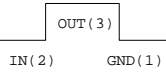
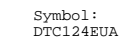
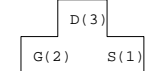
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Size	Document Number FX6		Rev 3A
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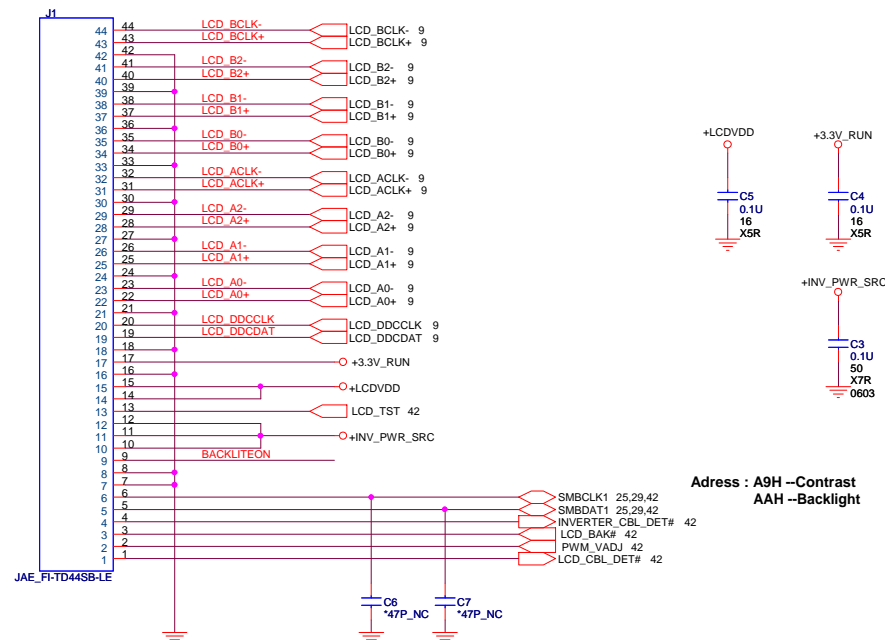
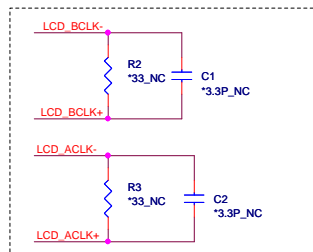
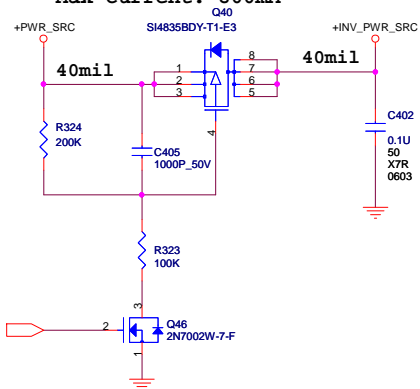
Title				
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Place Decoupling Cap close to GROUP2 each VDD pin as possible.



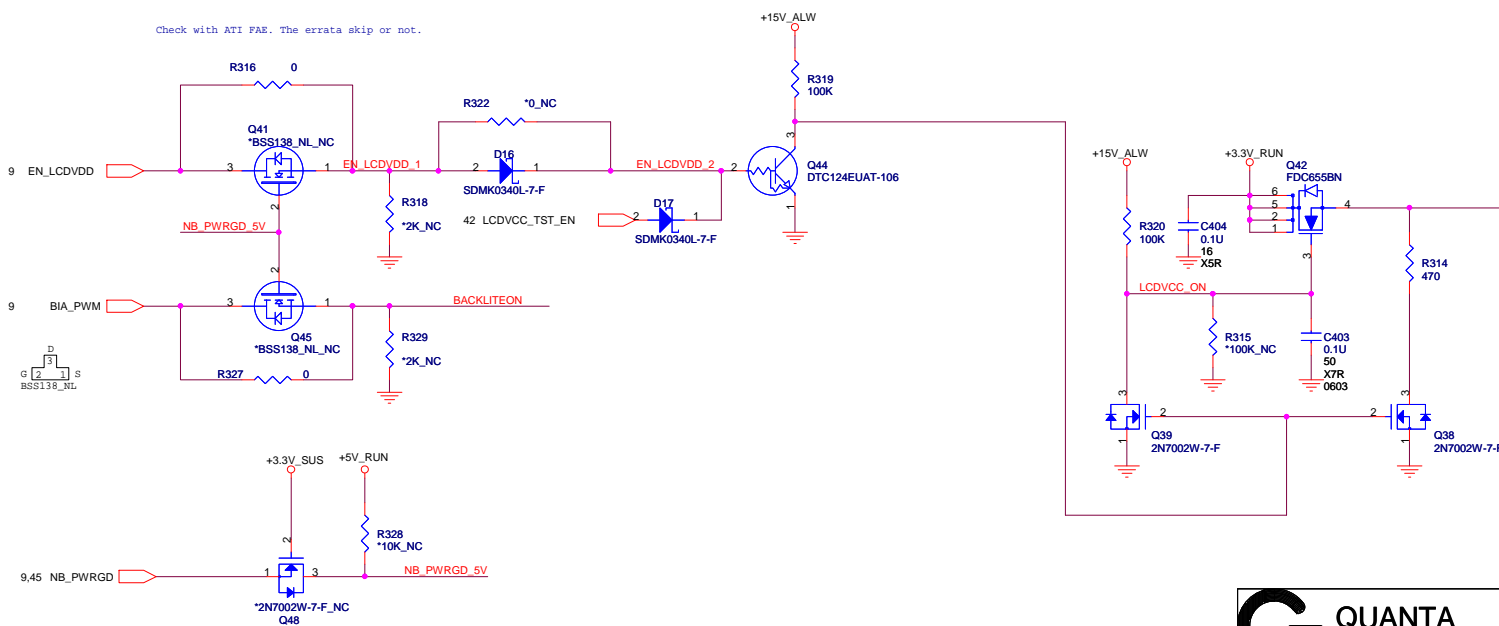


Design current: 560mA
Max current: 800mA



Adress : A9H --Contrast
AAH --Backlight

Check with ATI FAE. The errata skip or not.



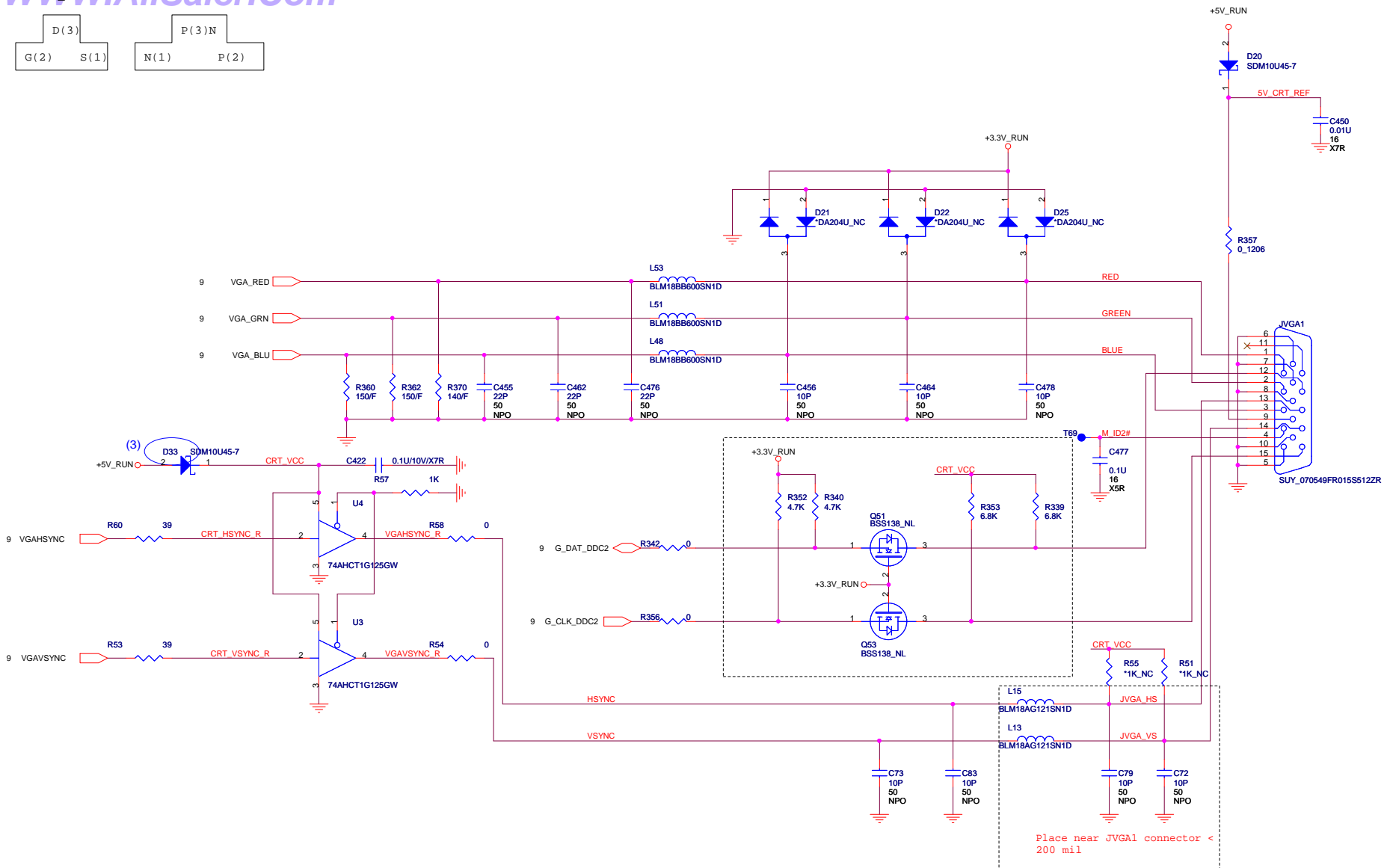
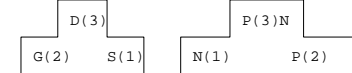
Title	LCD CONN,CK-SSCD
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Size	Document Number
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Title: CRT CONN

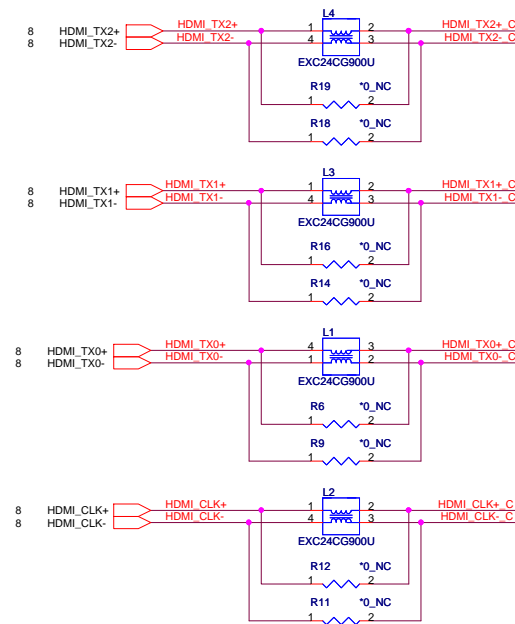
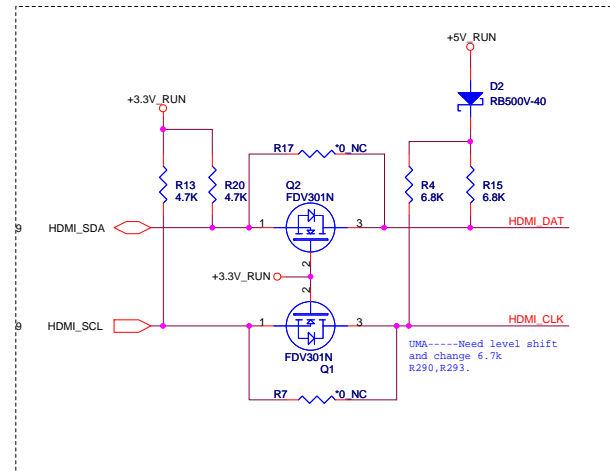
Size: Document Number FX6

Date: Wednesday, June 25, 2008

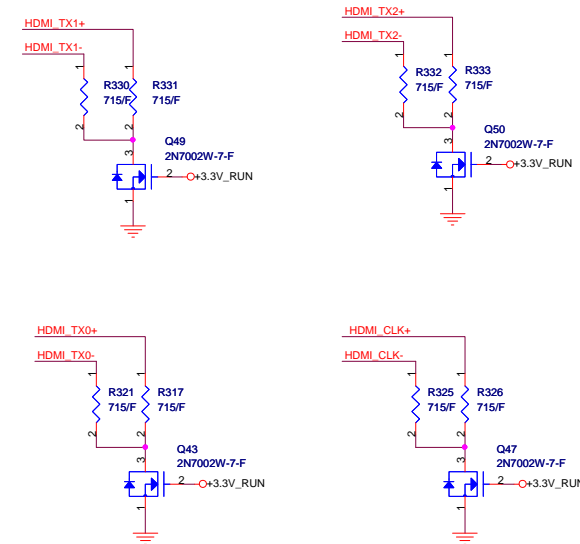
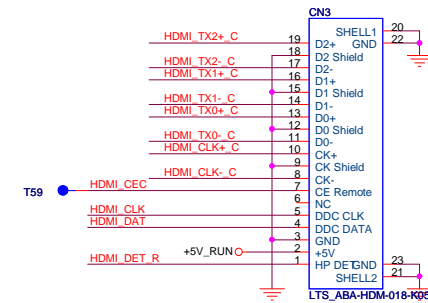
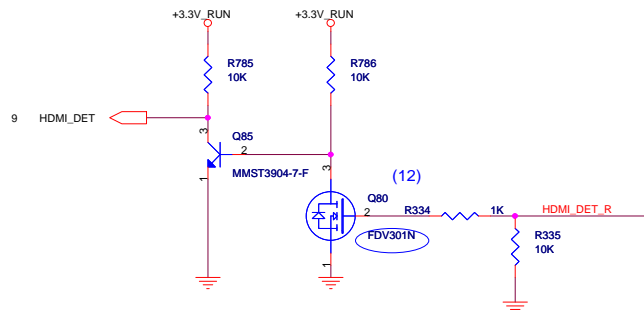
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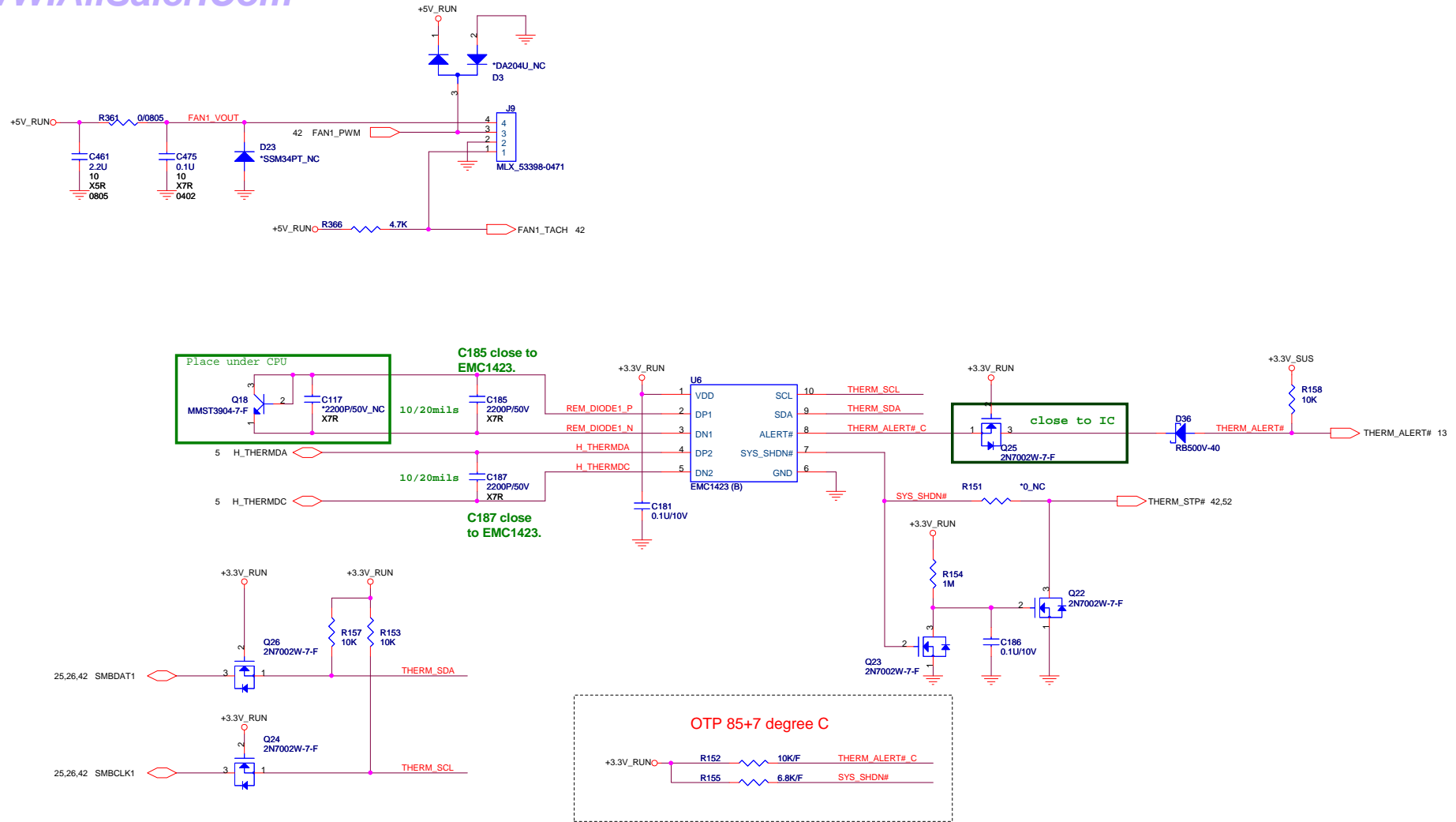
HDMI Connector



for EMI

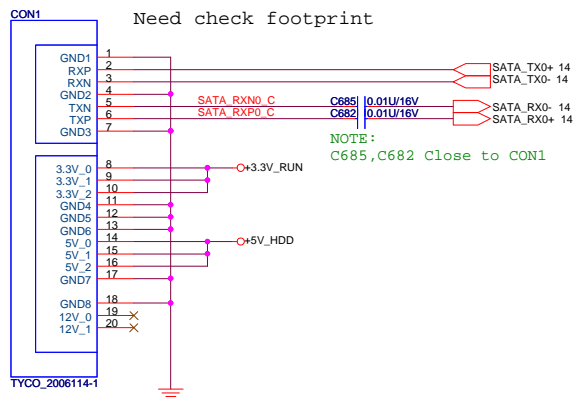
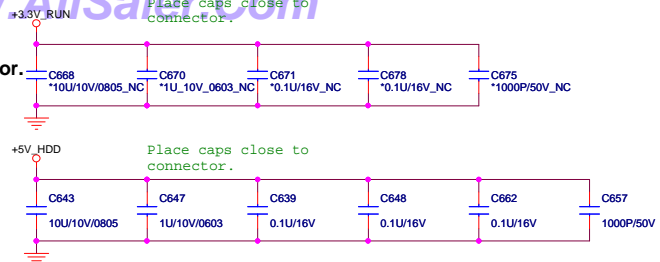


		QUANTA COMPUTER	
Title HDMI			
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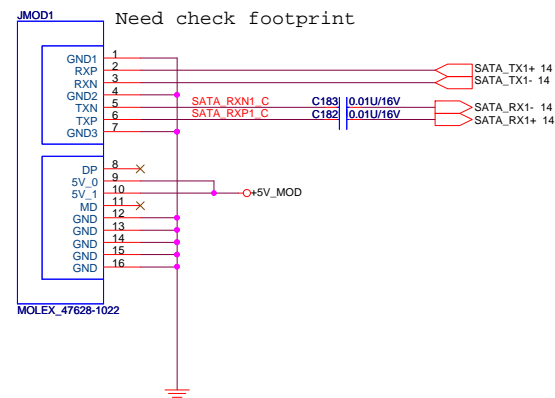
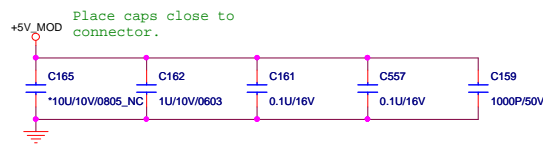


Title			FAN/THERMAL
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SATA Connector.

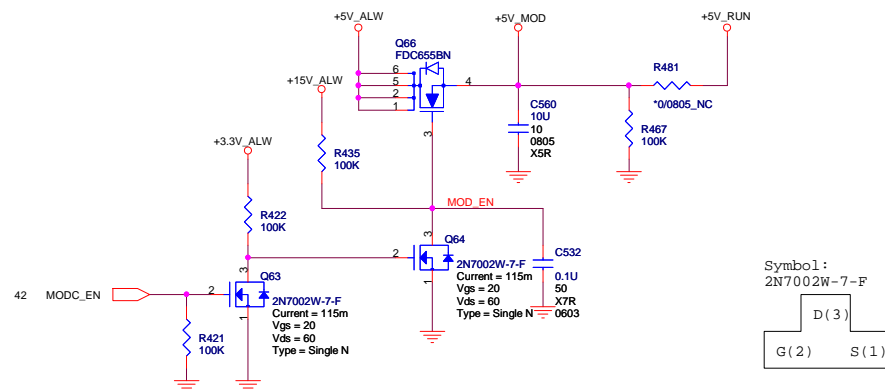
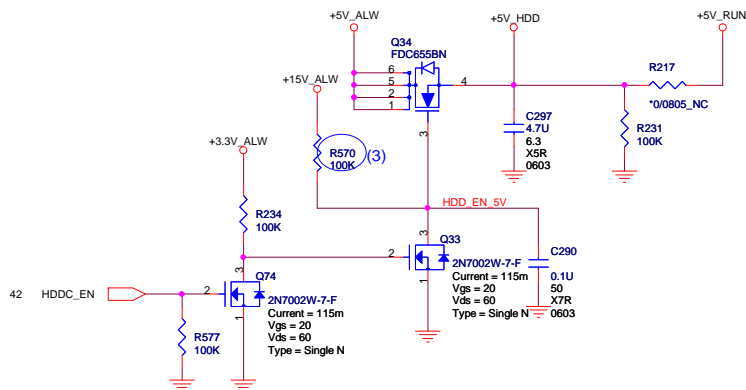


ODD Connector.



Design current: 1050mA
Max current: 1500mA

Design current: 700mA
Max current: 1000mA



QUANTA COMPUTER

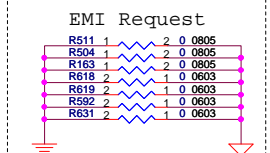
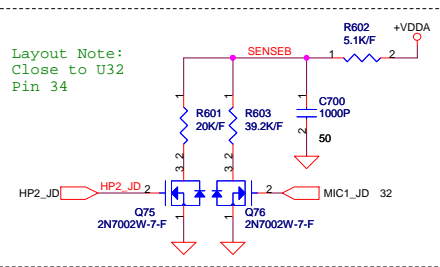
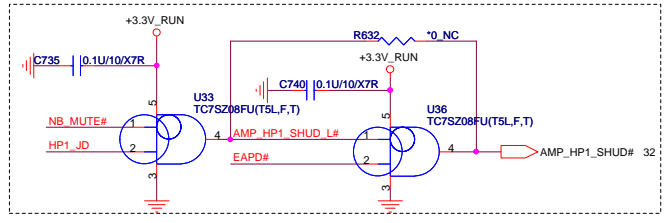
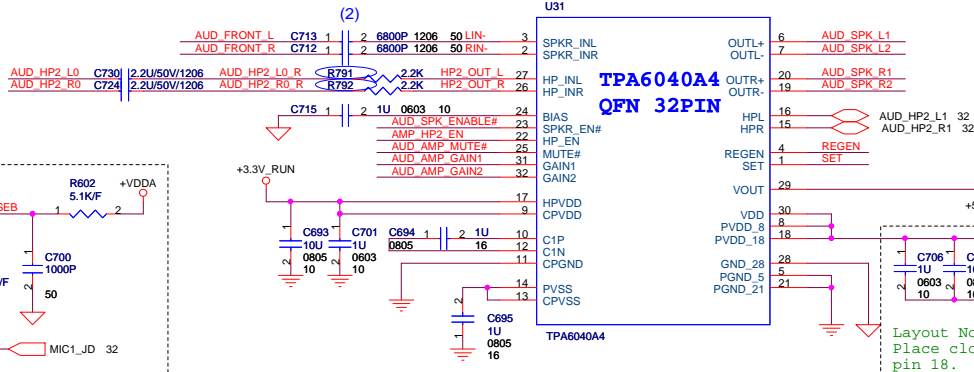
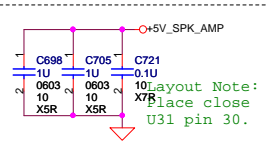
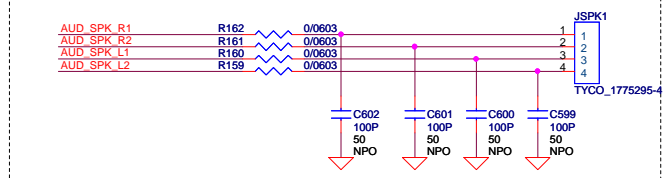
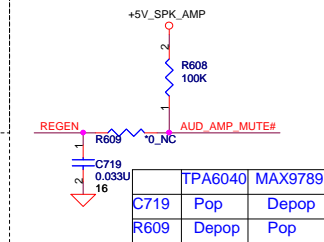
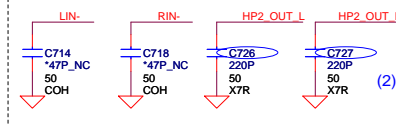
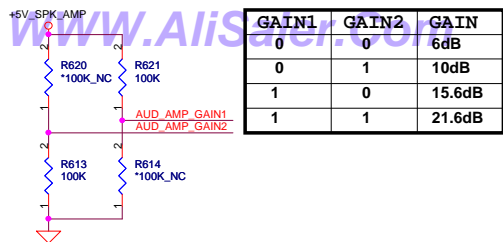
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Size: Document Number FX6

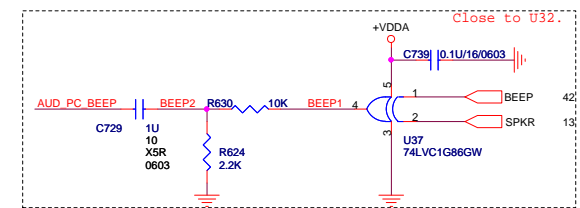
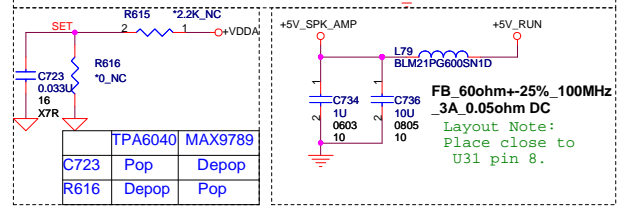
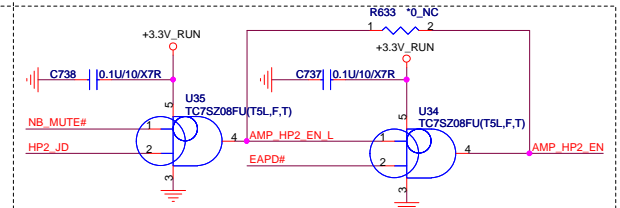
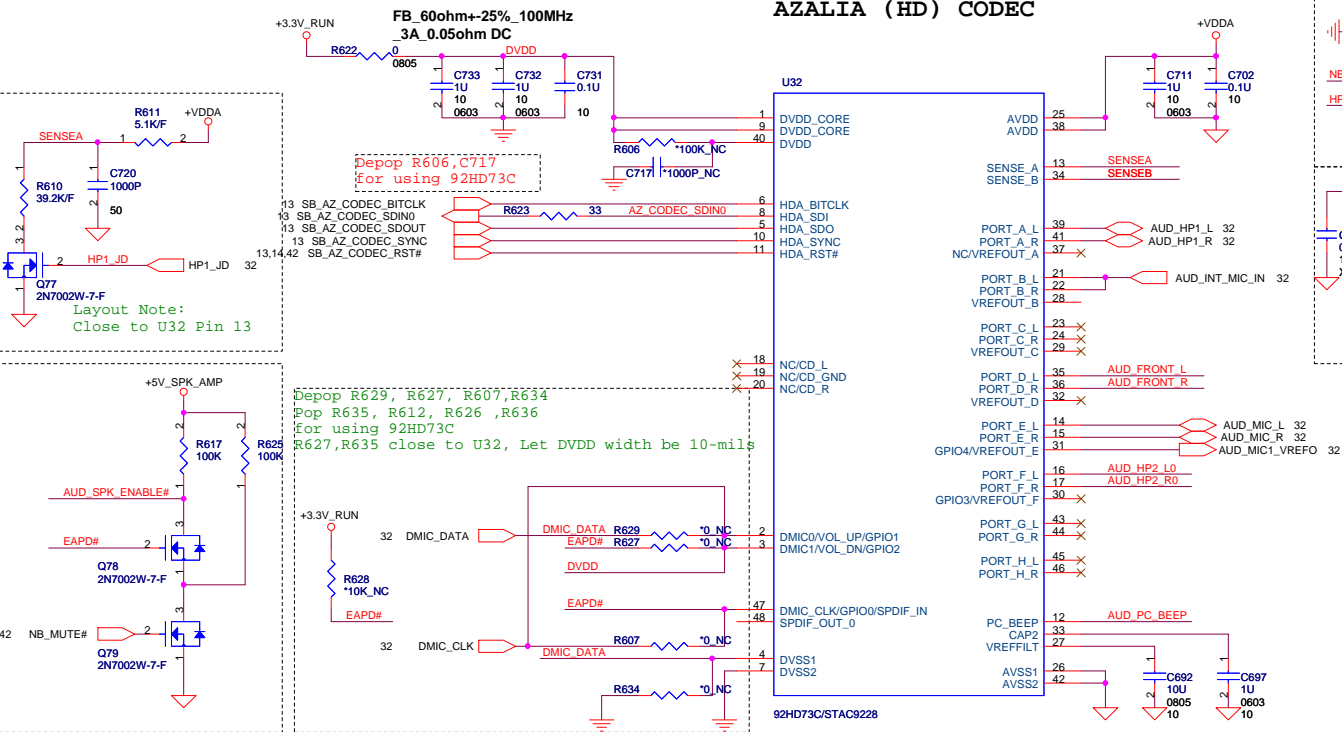
Date: Wednesday, June 25, 2008

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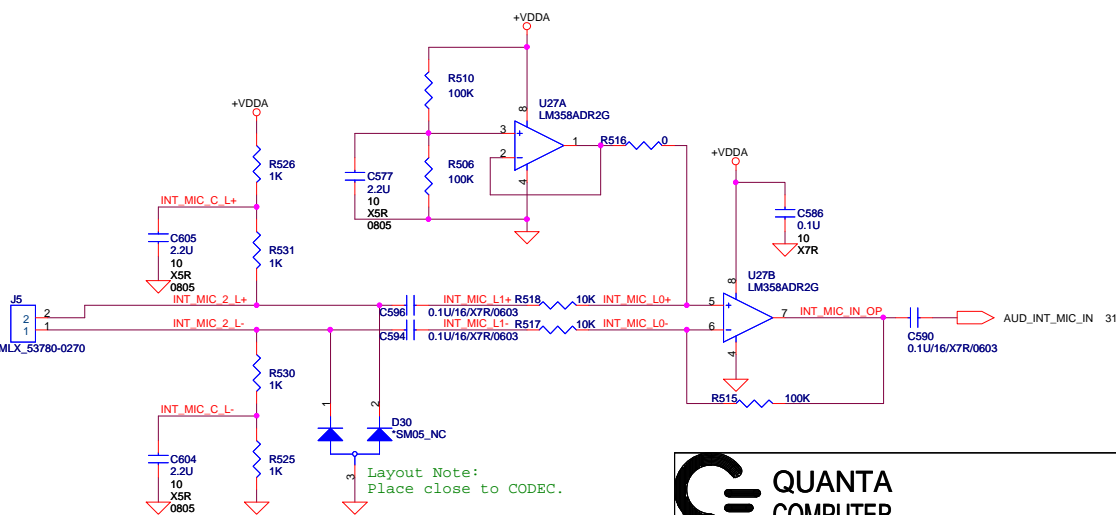
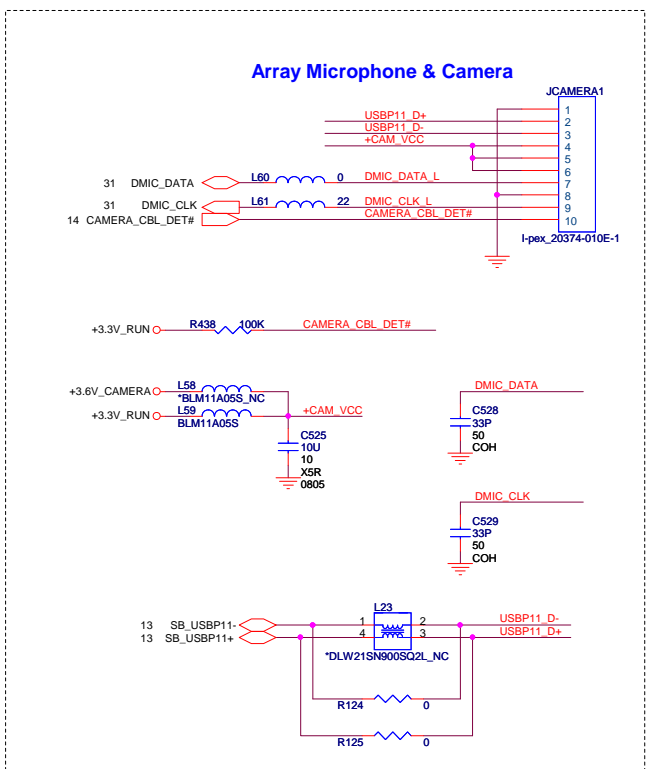
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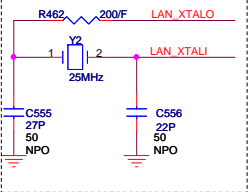
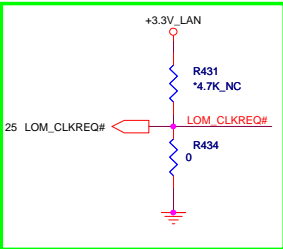
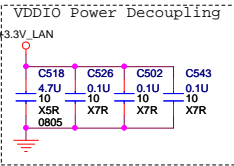
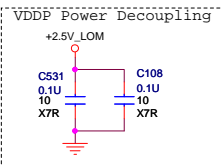
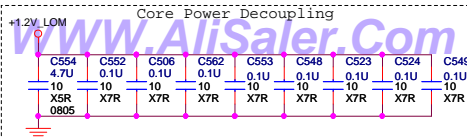
AZALIA (HD) CODEC



Title			AZALIA(HD) CODEC
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 <div> <div>QUANTA</div> <div>COMPUTER</div> </div>	
Title AUDIO CONN	
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LAN_DISABLE# is active high.

Table 1 - Component Stuffling Requirements

	INSTALL	NOT INSTALL
5787M	R479,R429,R407,R96,R103,R106,R120,R115,R108,Q67,C142,C145,C157,C158,R418,R464,R461,L68	R428,R425,R94,R101,R105,R122,R119,R111,R449,R408,R463,R460
5784	R428,R425,R94,R101,R105,R122,R119,R111,R449,R408,R463,R460	R479,R429,R407,R96,R103,R106,R120,R115,R108,Q67,C142,C145,C157,C158,R418,R464,R461,L68

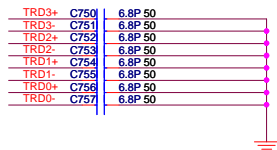
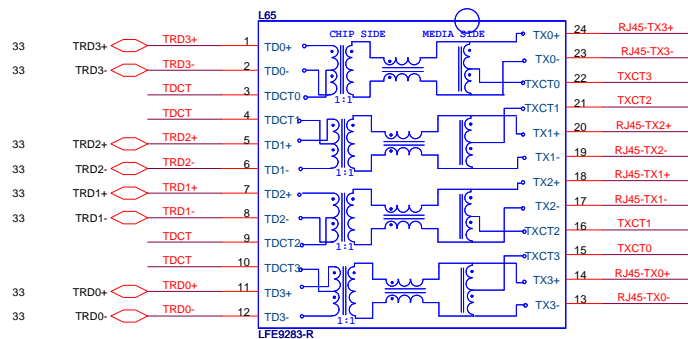
BCM5784M/5787M
10mm x 10mm
68-Pin QFN

Note:thermal pad

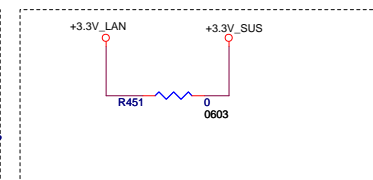
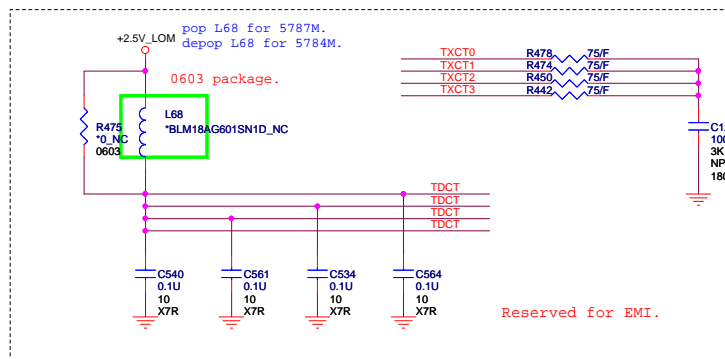
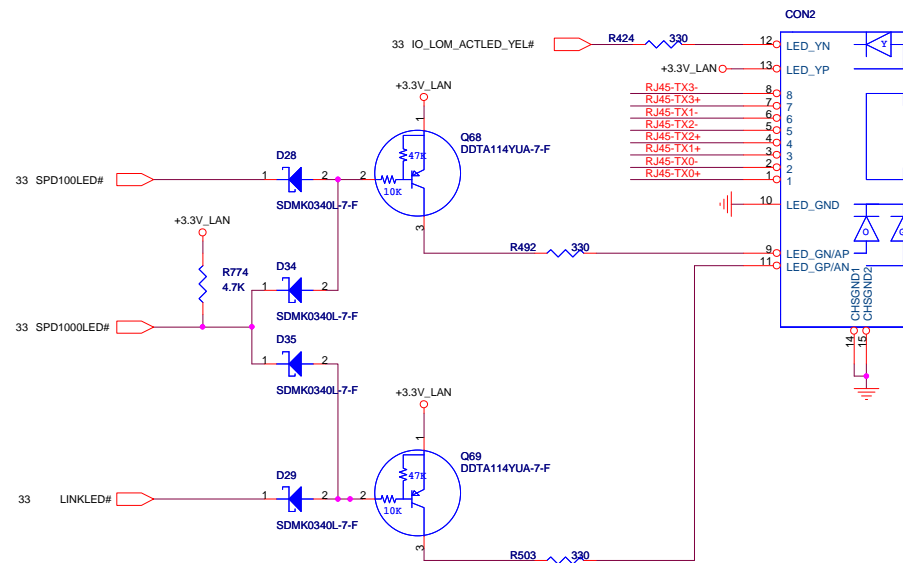
5784M	5787M
R439	39k
R440	20k

Title		LAN(BCM5784M/5787M)	
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CustomFX6			
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TRANSFORM



RJ-45 Connector



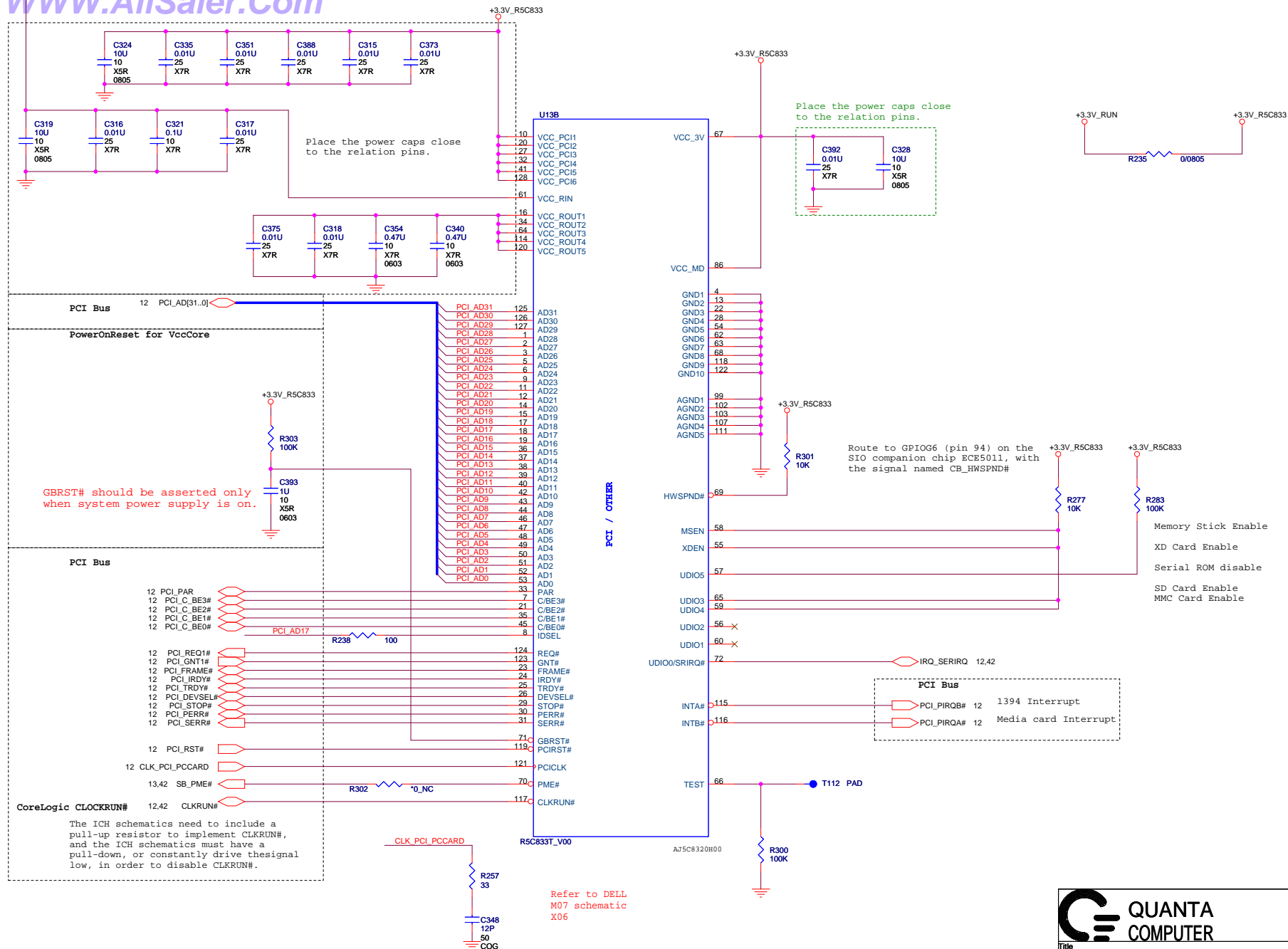
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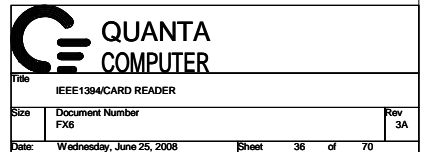
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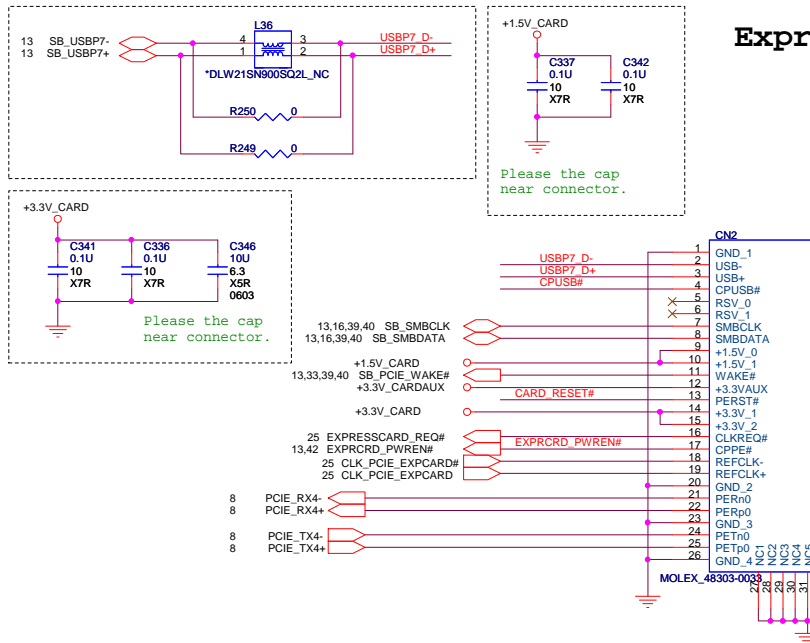
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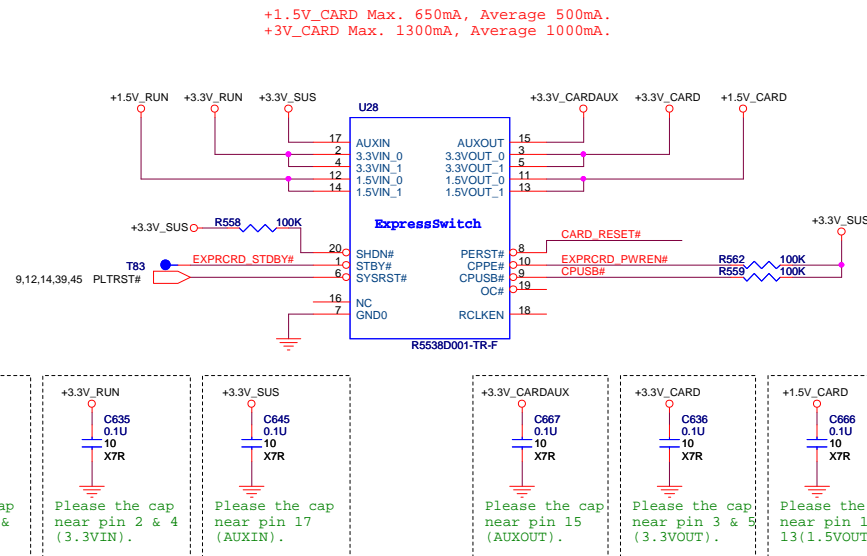




Express Card



PCI-Express TX and RX direct to connector.



EXPRESS

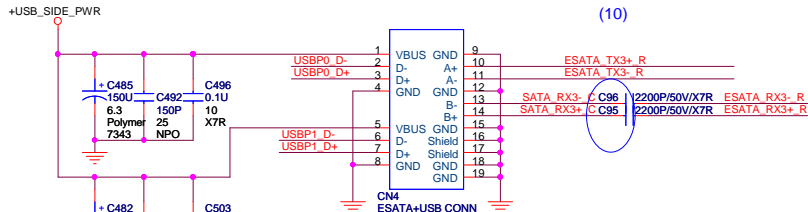
Size Document Number

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Side External USBX2



(7) PJP14

+5V_ALW

FS2 *455/5A_NC

42 USB_SIDE_EN#

C494 0.1uF 10 X7R

C493 10uF X5R 0805

(3) (4)

U7

IN

EN1#

EN2#

GND

OUT1

OC1#

OUT2

OC2#

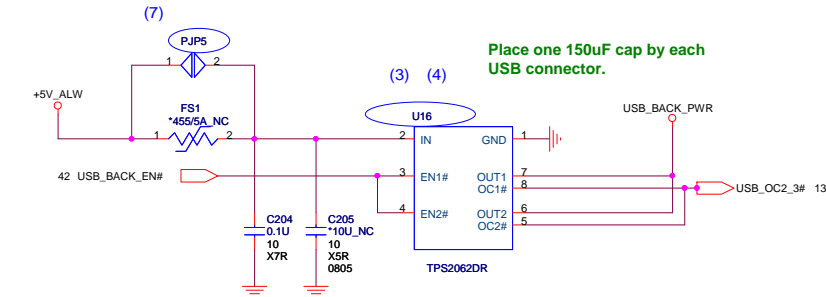
TPS2062DR

+USB_SIDE_PWR

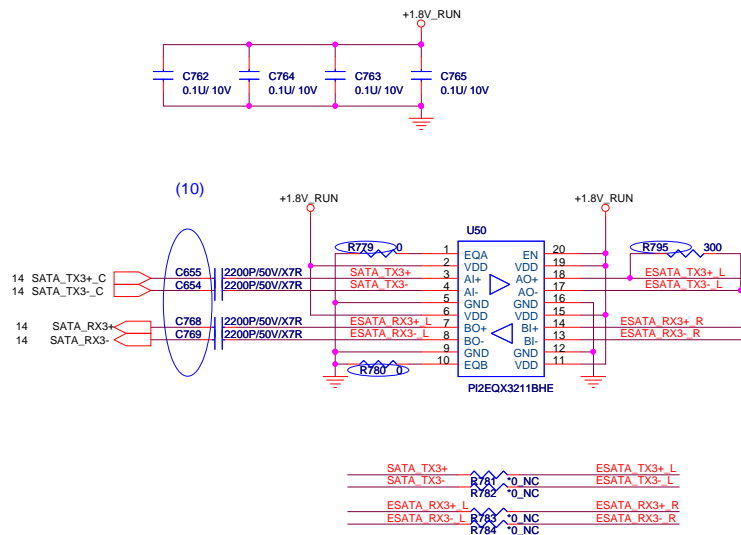
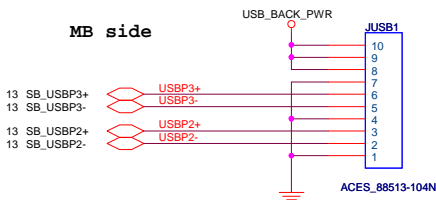
USB_OC0_1# 13

Place one 150uF cap by each USB connector.

Place one 150uF cap by each USB connector.



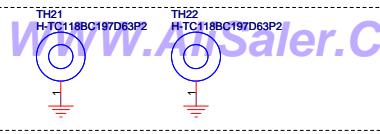
MB side



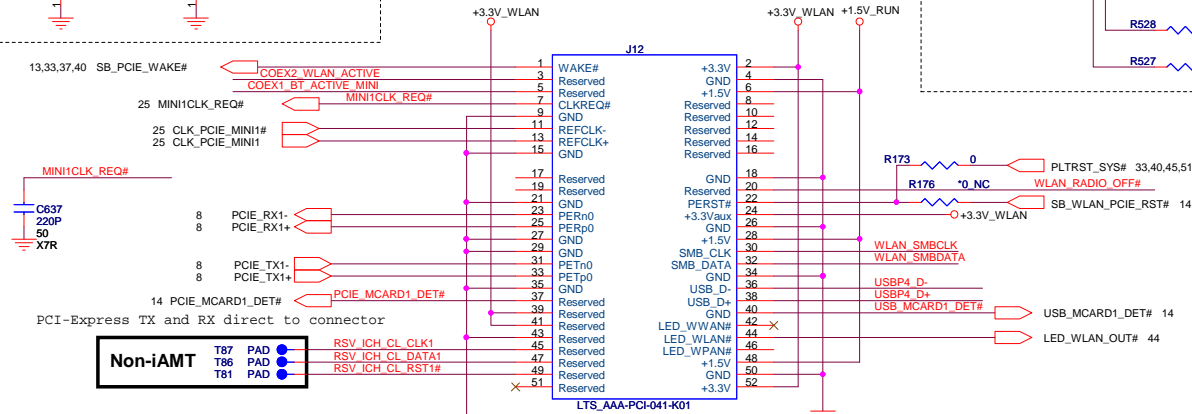
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3

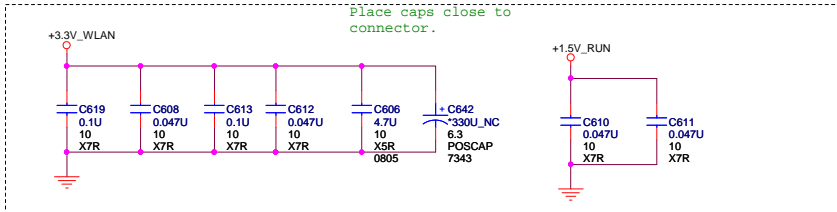


MiniCard WLAN connector

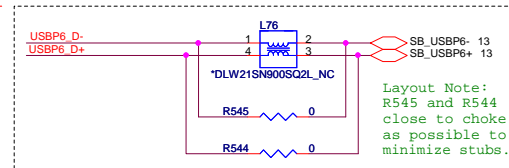
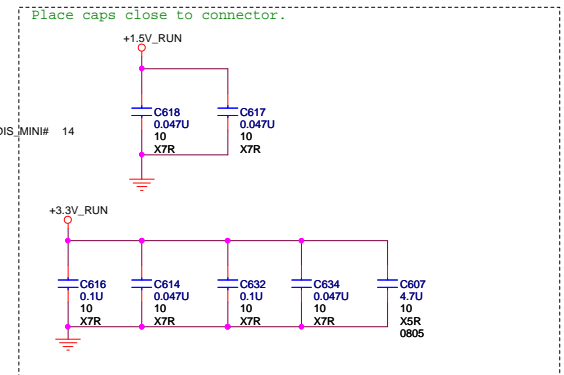
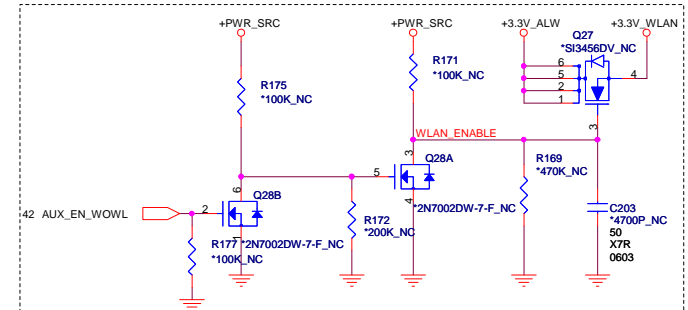
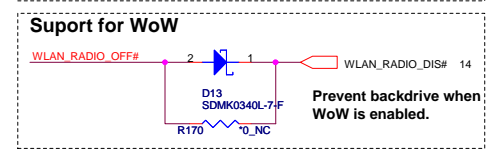
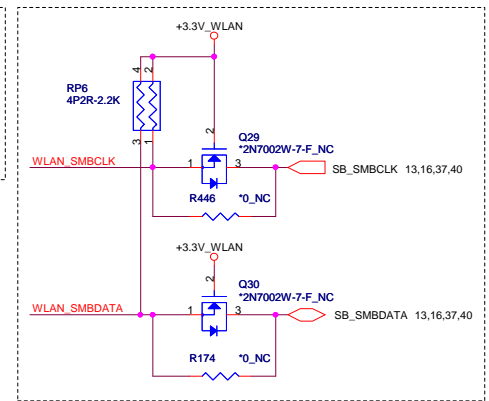
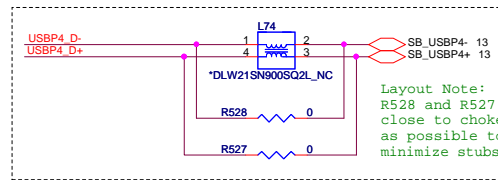
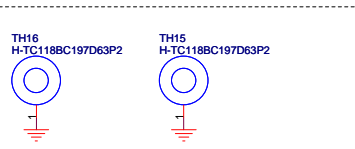
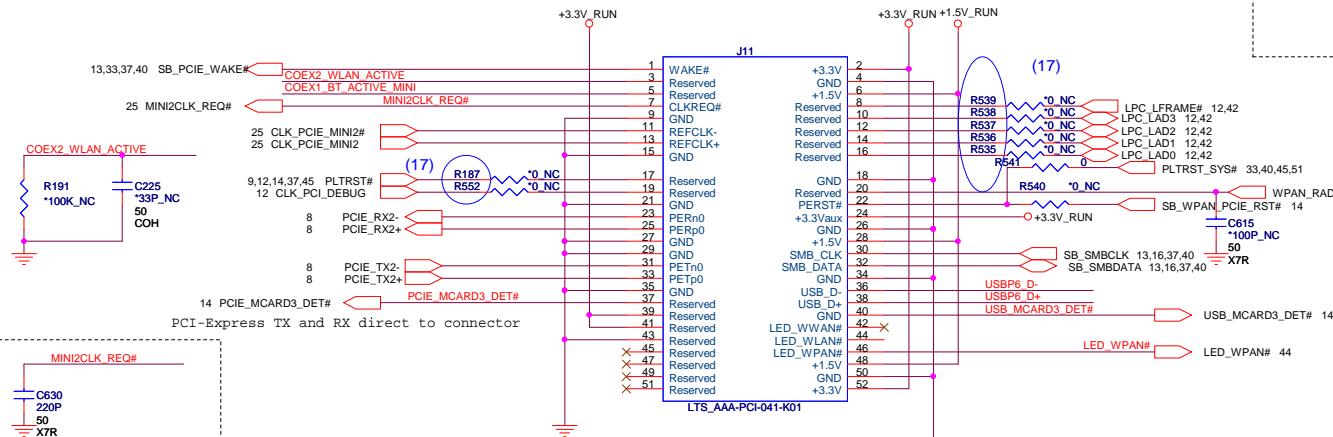


DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81



MiniCard WPAN connector



QUANTA COMPUTER

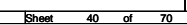
Title: MINI CARD

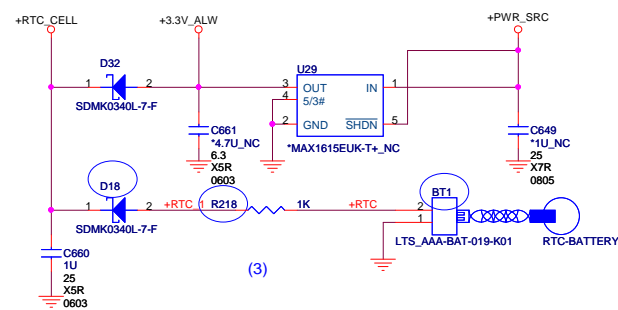
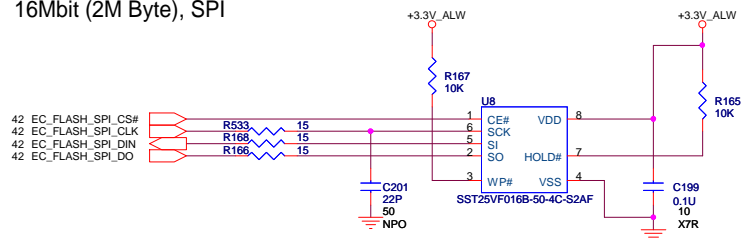
Size: Document Number FX6

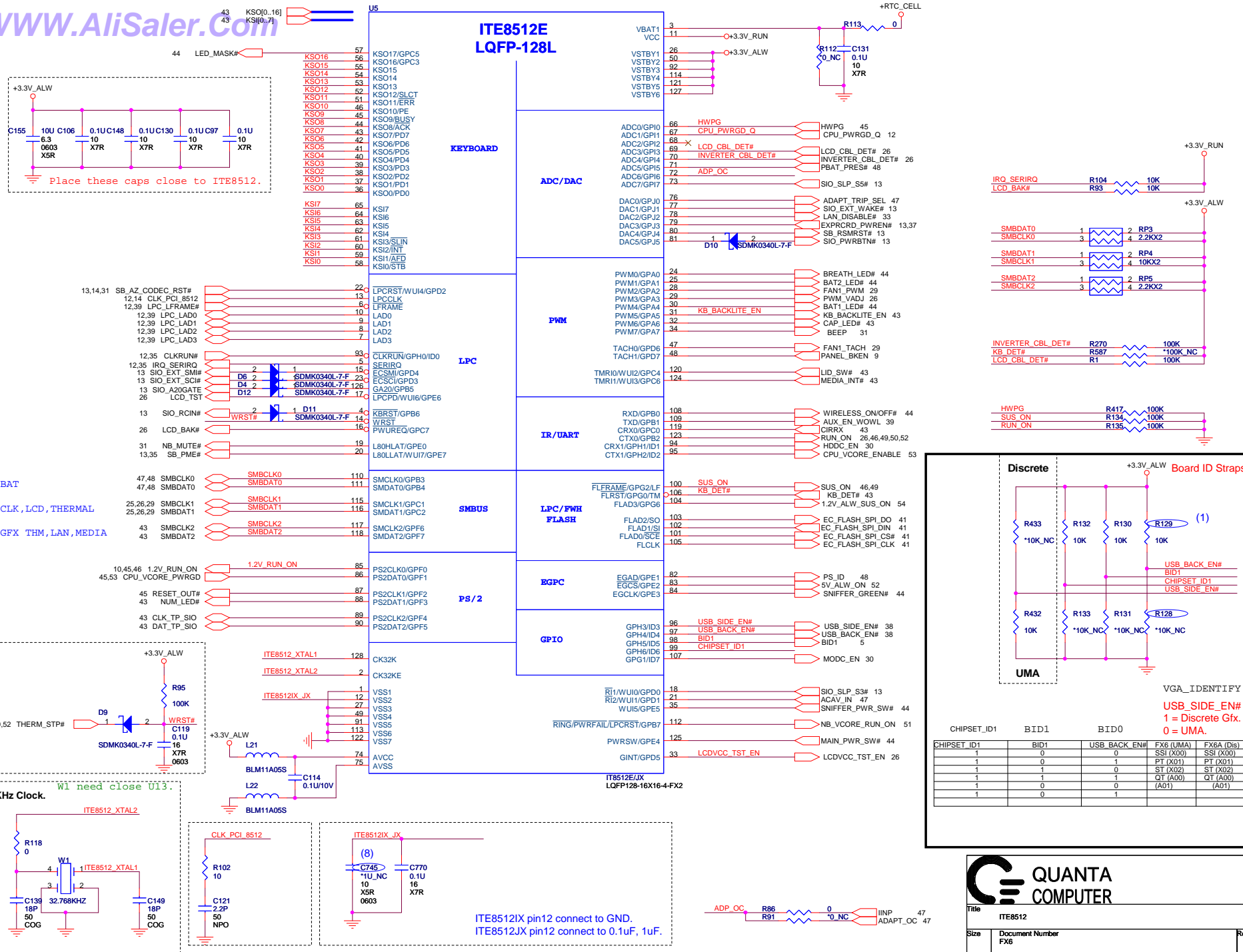
Date: Wednesday, June 25, 2008

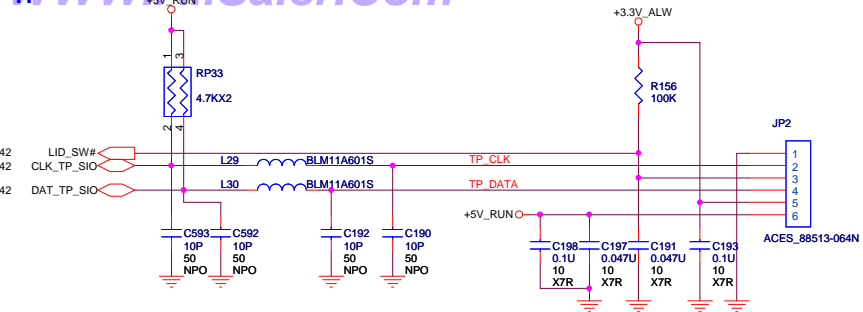
Sheet: 39 of 70

Rev: 3A

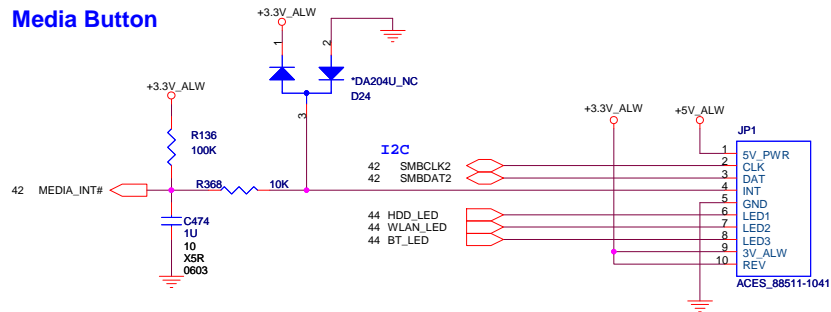




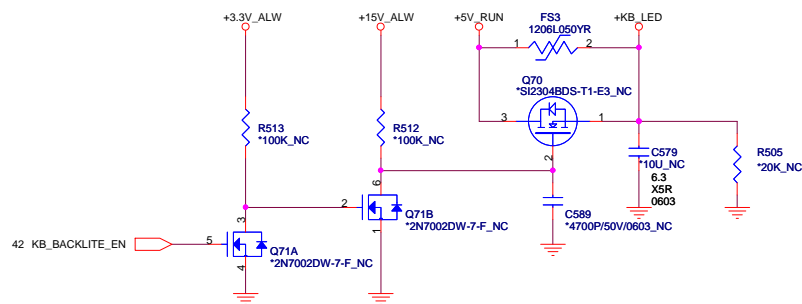
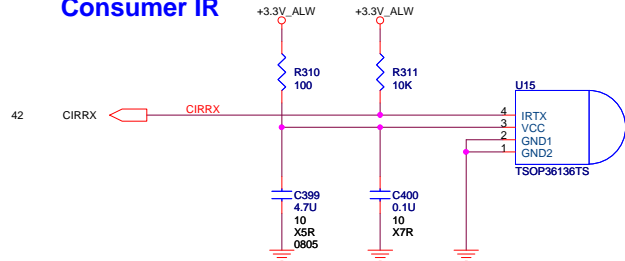




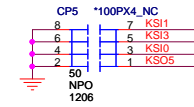
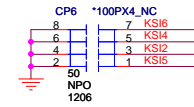
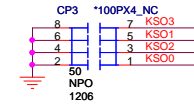
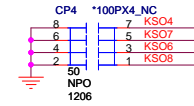
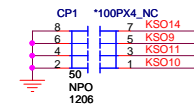
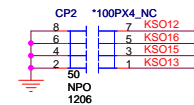
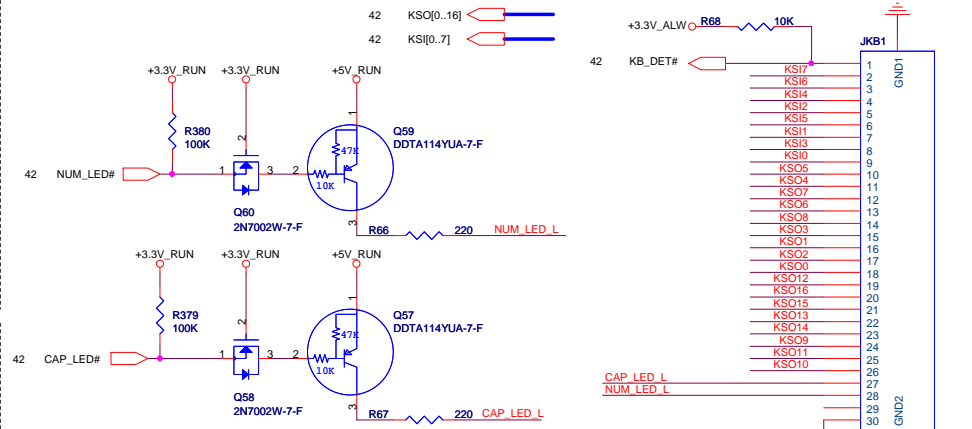
Media Button



Consumer IR

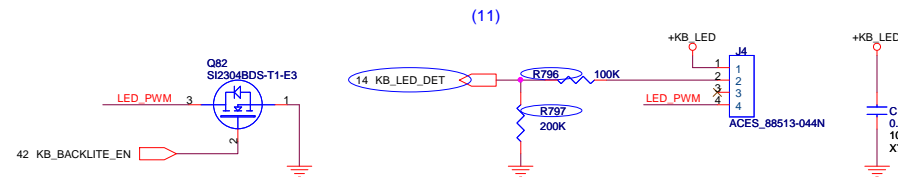


KEYBOARD CONNECTOR

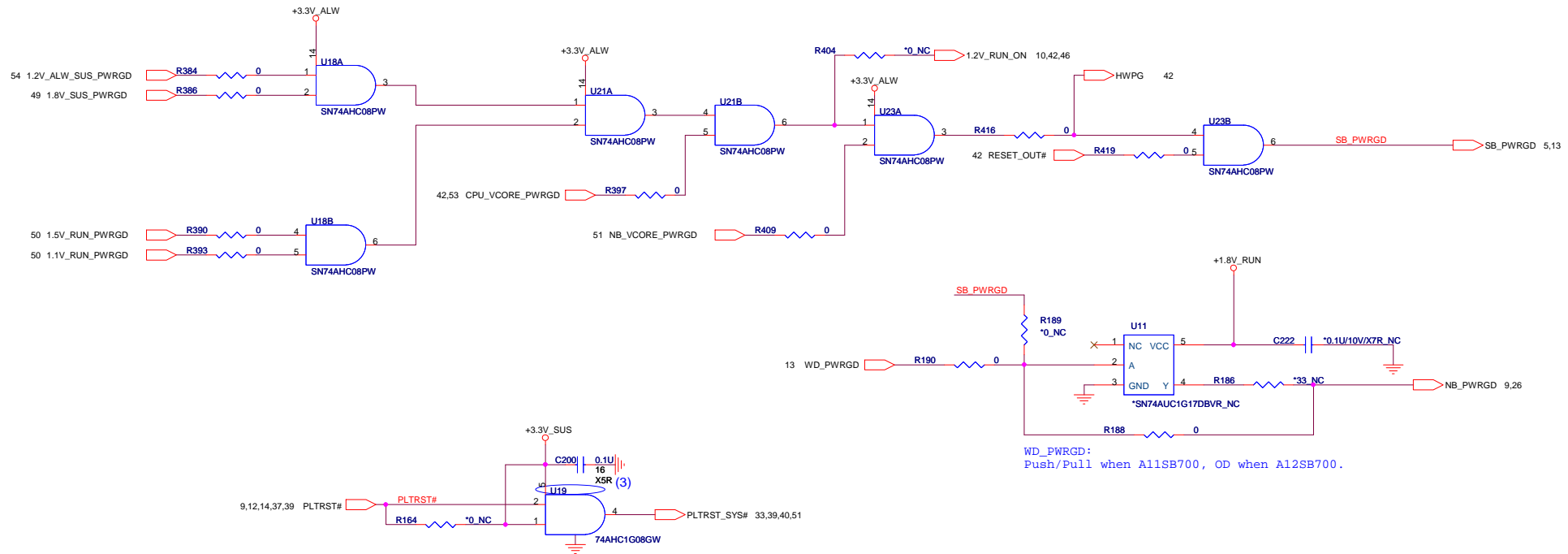


100P CAPS CLOSE TO JKB1

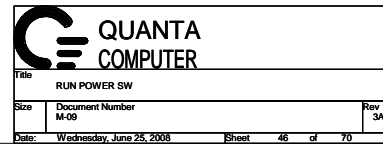
Key board Illumination

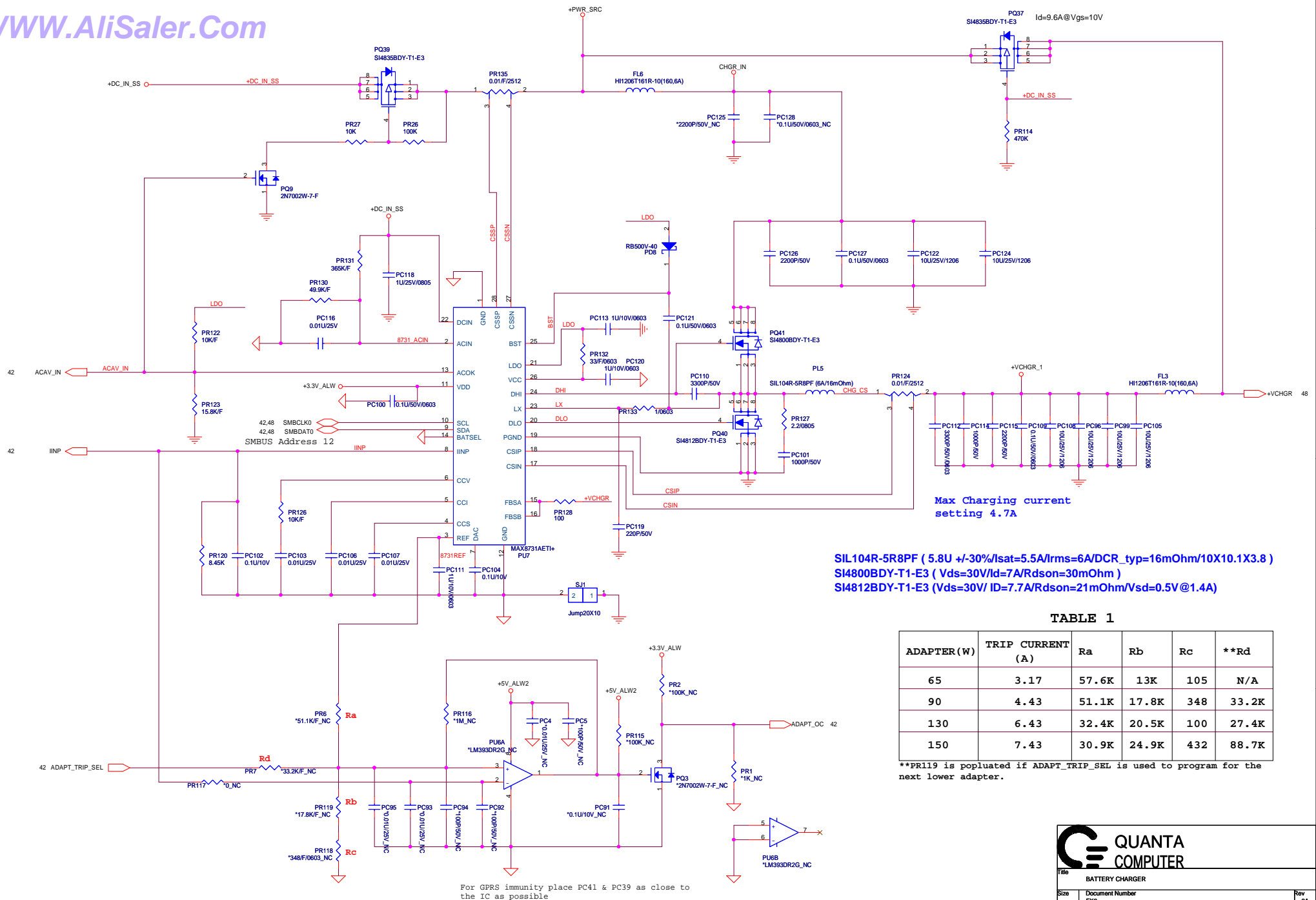


Title			TP/KB/CIR/BT
Size	Document Number	Rev	
FX6		3A	
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Title			System Reset Circuit
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FX6		3A	
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Max Charging current setting 4.7A

SIL104R-5R8PF (5.8U +/-30%/Isat=5.5A/Irms=6A/DCR_typ=16mOhm/10X10.1X3.8)
 SI4800BDY-T1-E3 (Vds=30V/Id=7A/Rdson=30mOhm)
 SI4812BDY-T1-E3 (Vds=30V/ ID=7.7A/Rdson=21mOhm/Vsd=0.5V@1.4A)

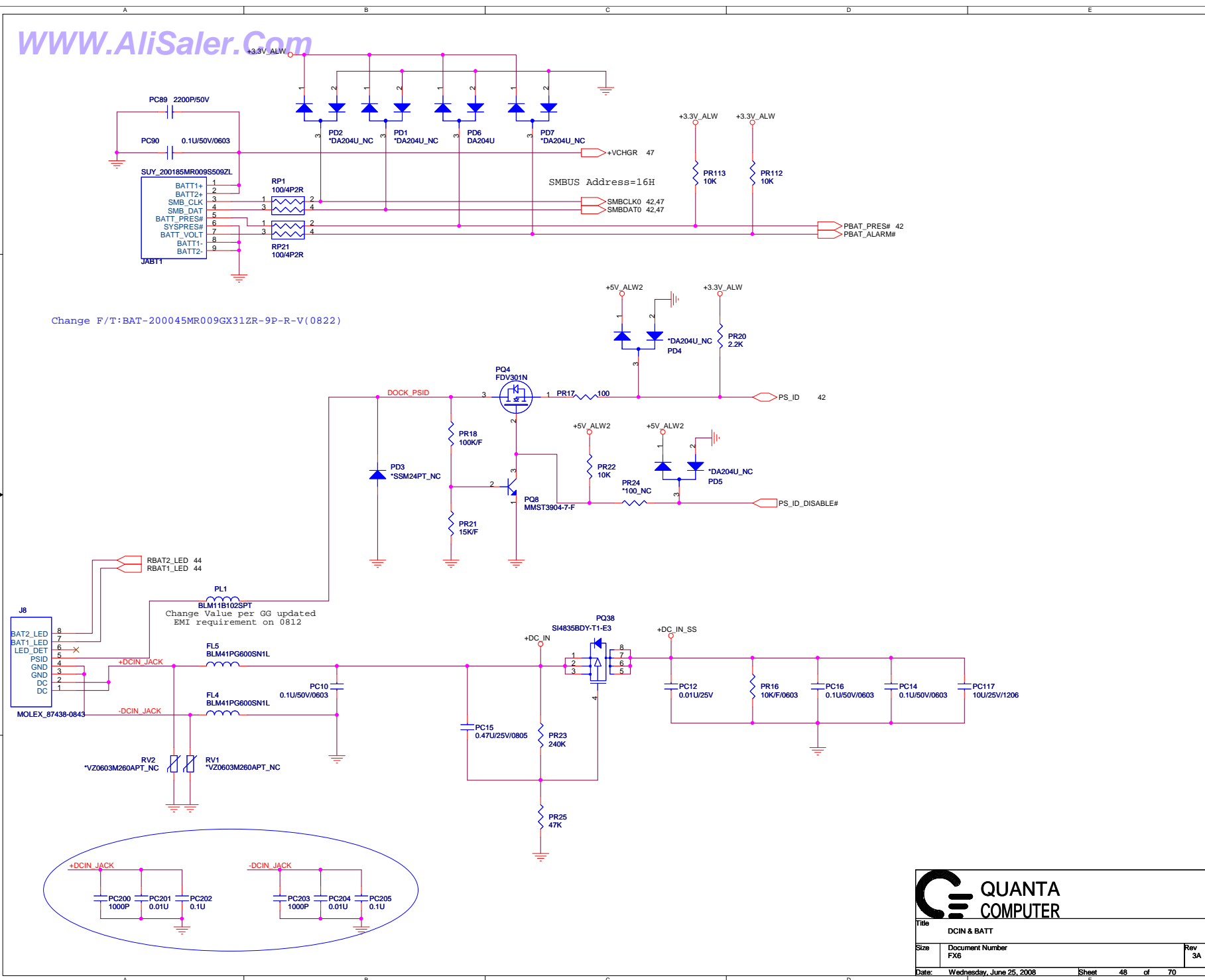
TABLE 1

ADAPTER (W)	TRIP CURRENT (A)	Ra	Rb	Rc	**Rd
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K

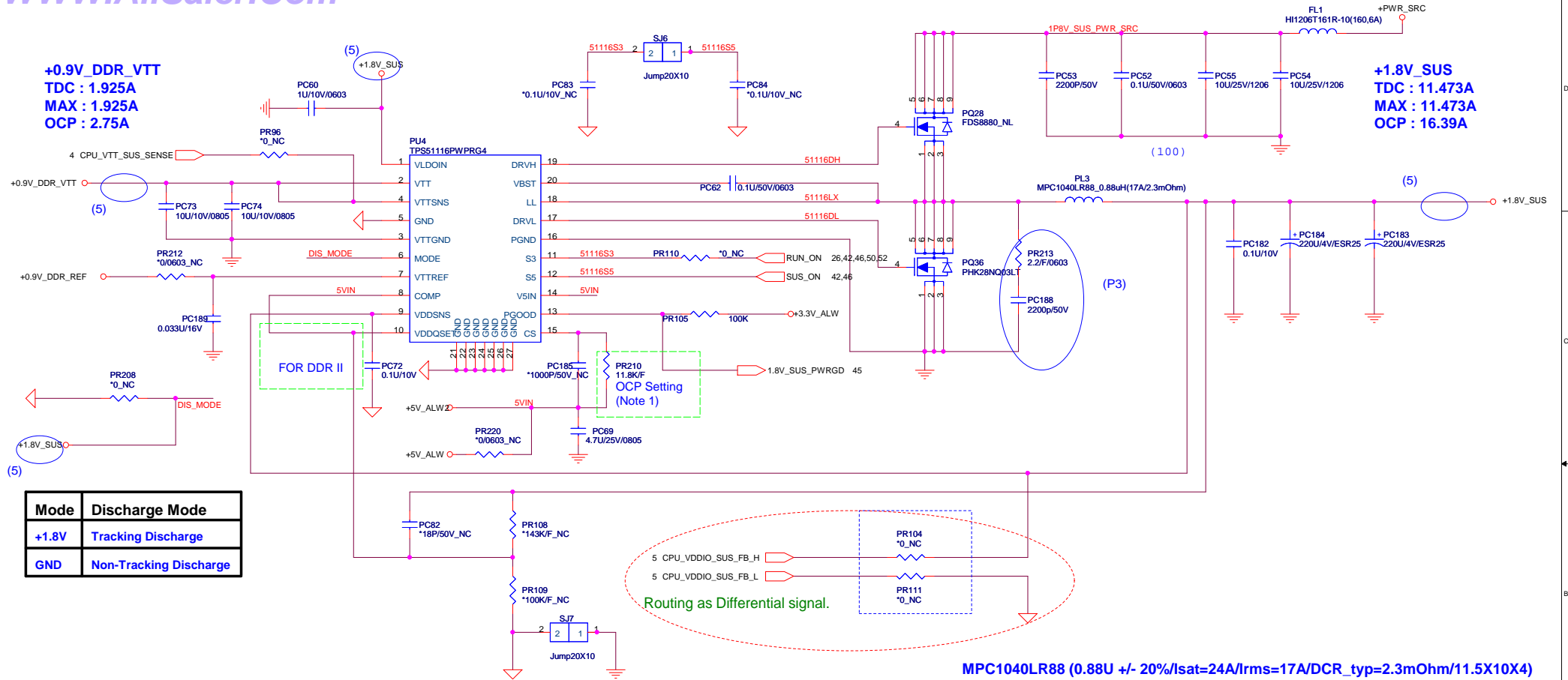
**PR119 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

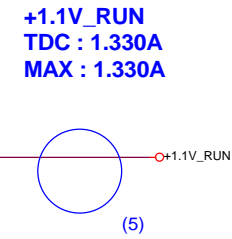
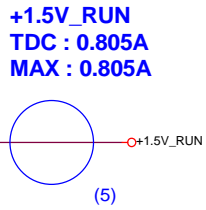
QUANTA COMPUTER	
File	BATTERY CHARGER
Size	Document Number FX6
Date	Wednesday, June 25, 2008
Sheet	47 of 70
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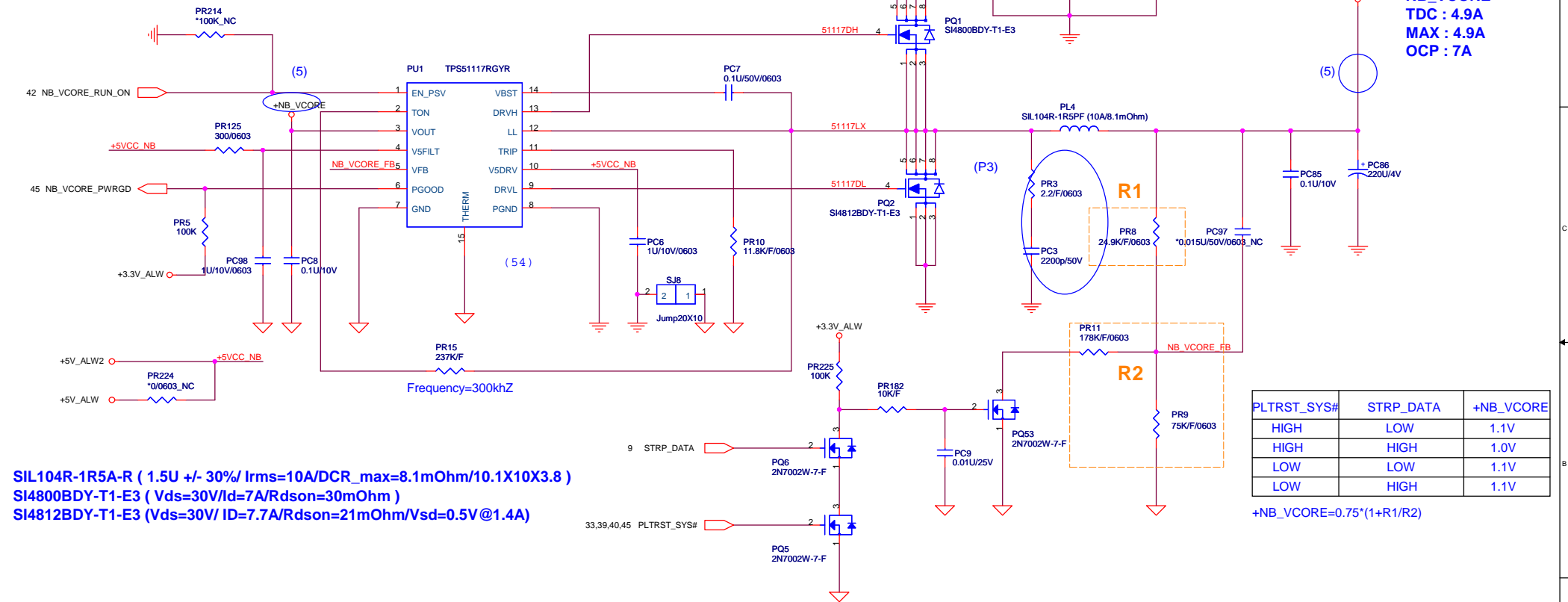
Change F/T:BAT-200045MR009GX31ZR-9P-R-V(0822)




Title		
DCIN & BATT		
Size	Document Number	Rev
FX6		3A
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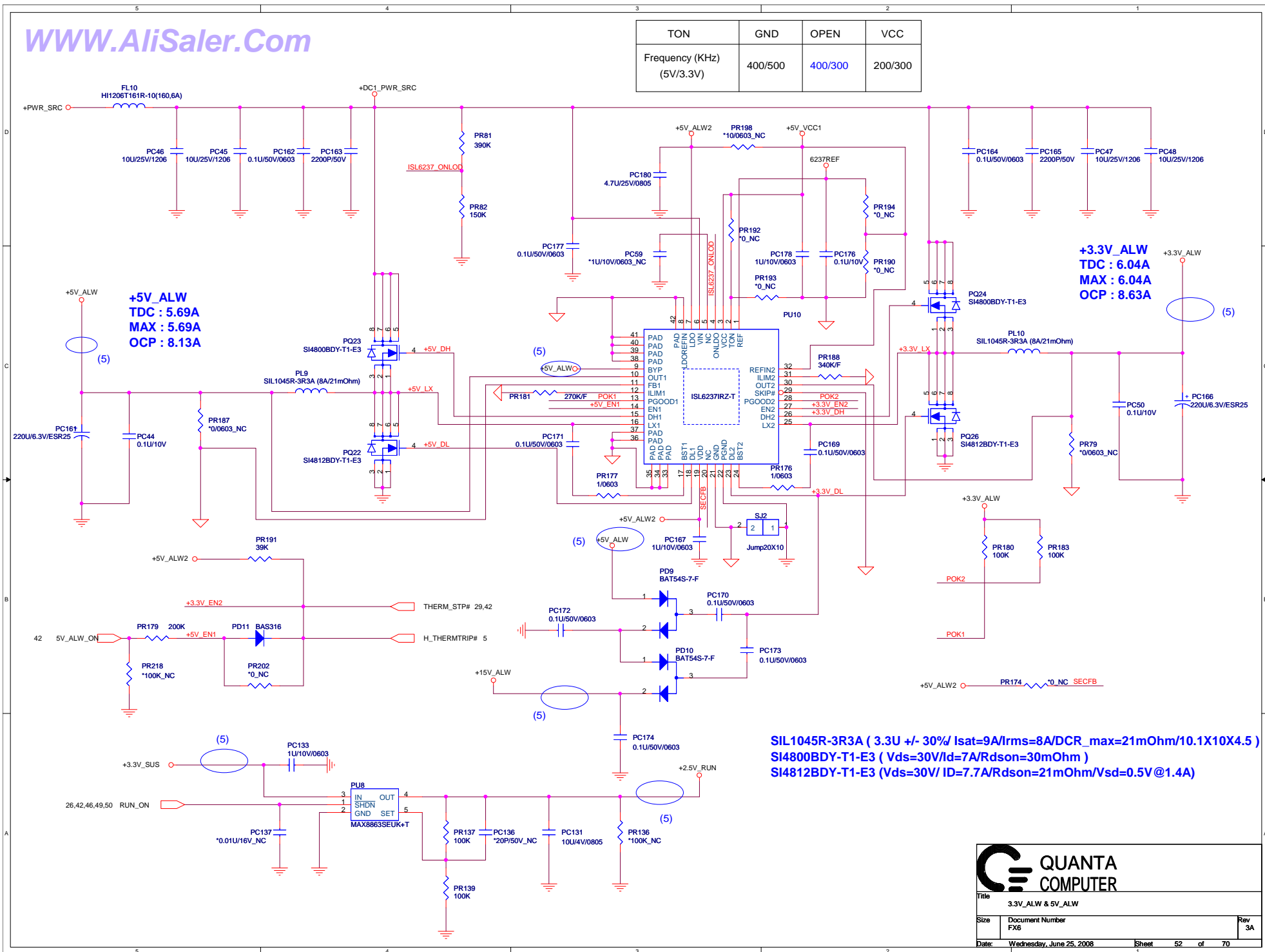






SIL104R-1R5A-R (1.5U +/- 30%/ Irms=10A/DCR_max=8.1mOhm/10.1X10X3.8)
 SI4800BDY-T1-E3 (Vds=30V/Id=7A/Rdson=30mOhm)
 SI4812BDY-T1-E3 (Vds=30V/ ID=7.7A/Rdson=21mOhm/Vsd=0.5V@1.4A)

 <div>QUANTA COMPUTER</div>	
Title: 3.3V_ALW & 5V_ALW	
Size	Document Number FX6
Date: Wednesday, June 25, 2008	Sheet 52 of 70 Rev 3A



ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

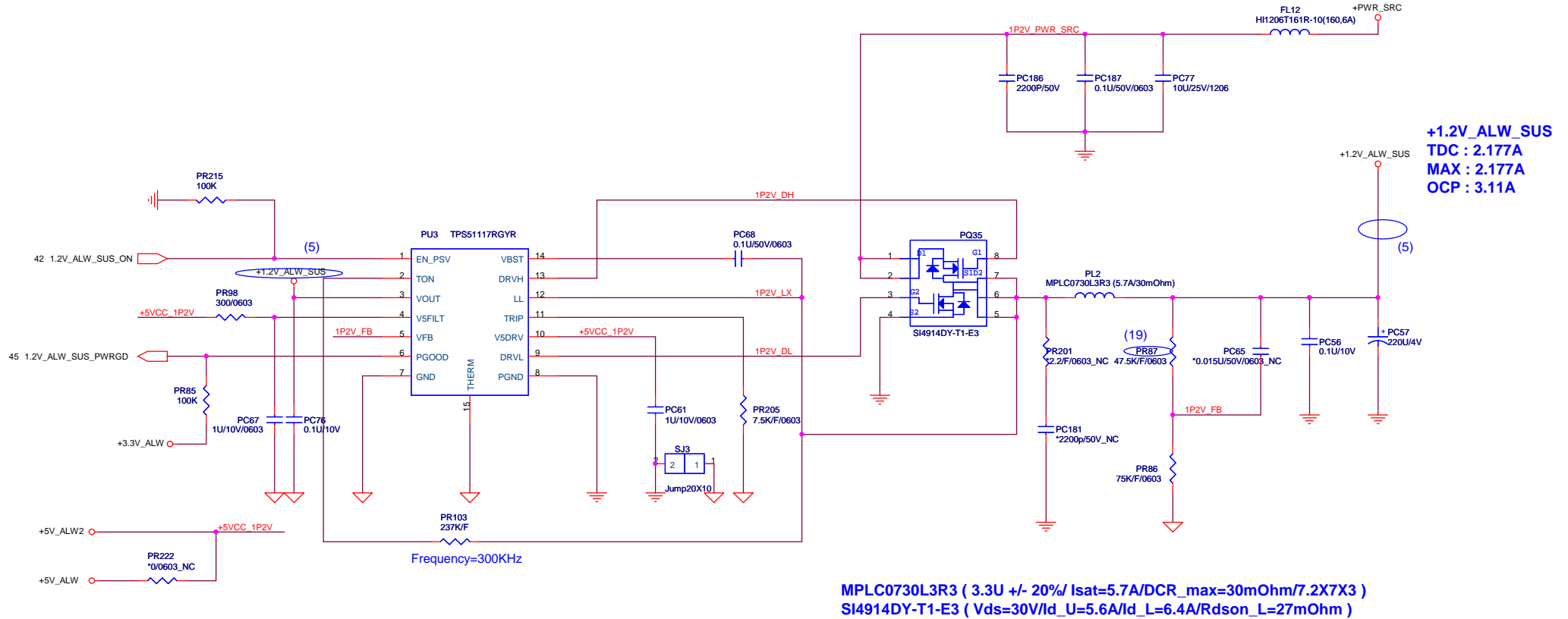
CPU_VDDNB_RUN
TDC : 2.1A
OCP : 3A


Pin 49 is GND Pin

ISL6265HRTZ-T




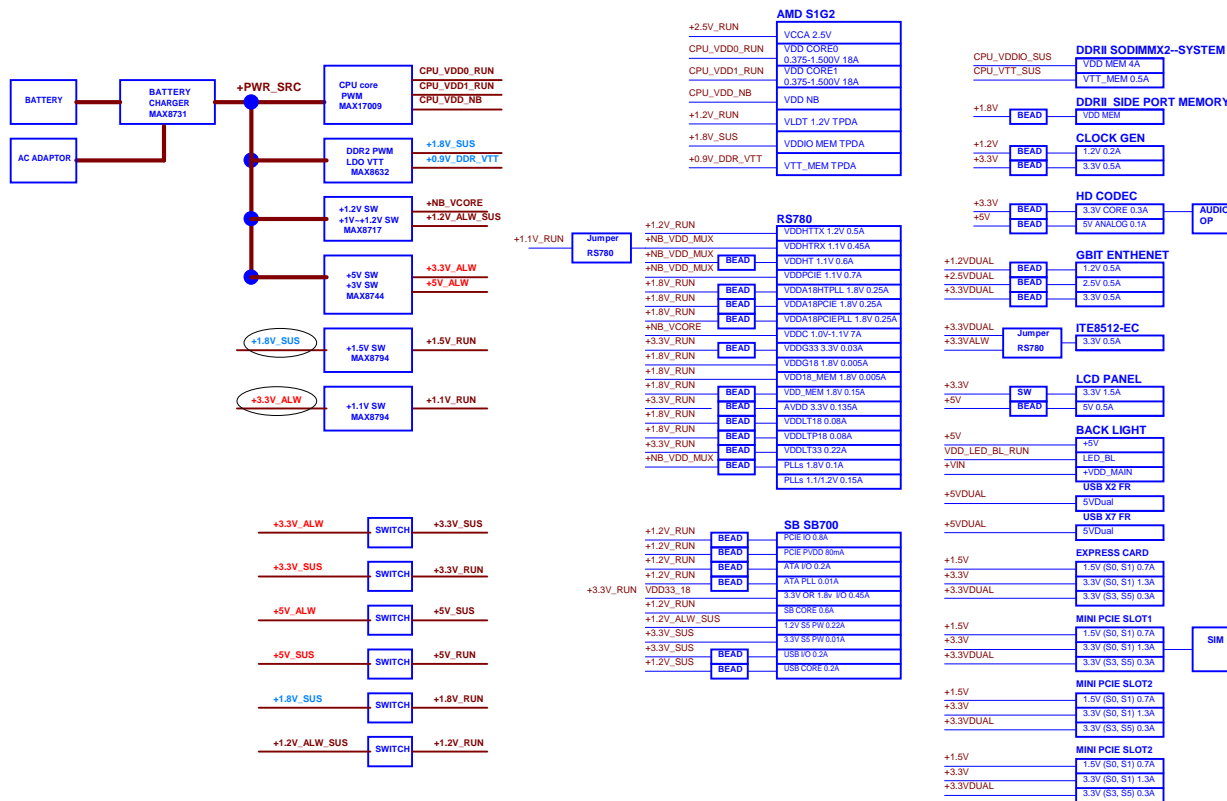
CPU_CORE_POWER		
File	Document Number	Rev
Size	FX8	3A
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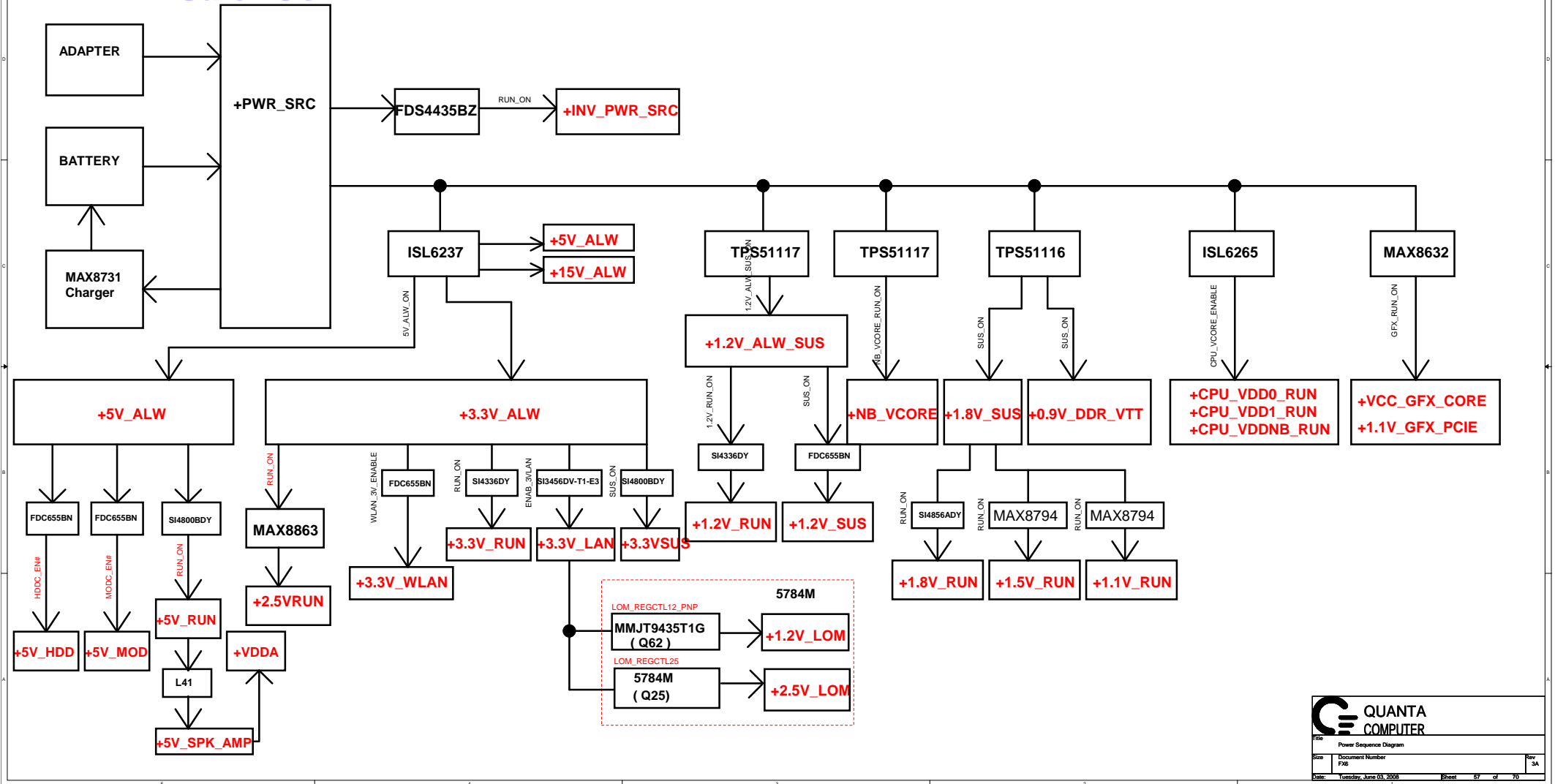


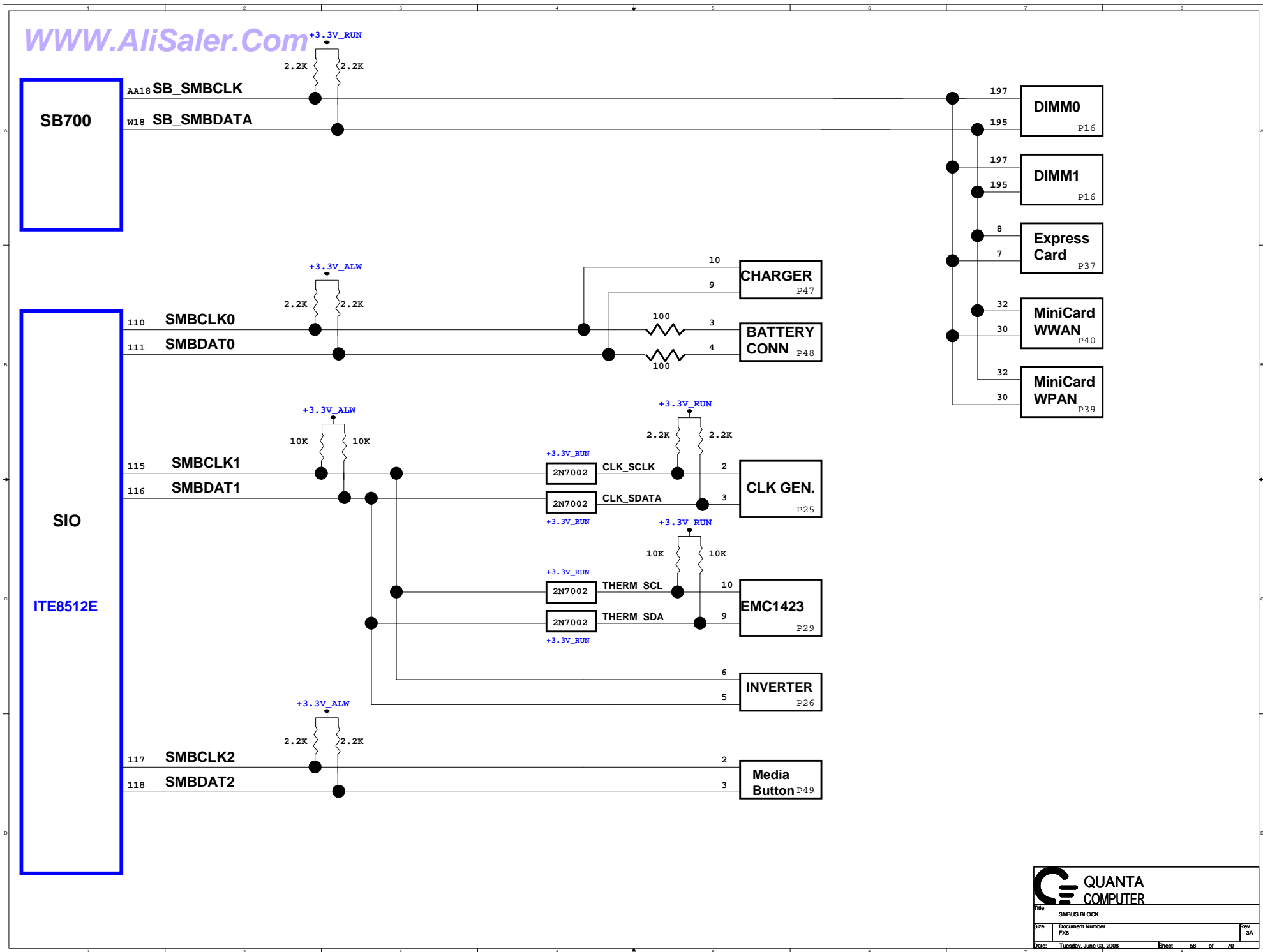
 QUANTA COMPUTER			
Title	1.2V_ALW_SUS		
Size	Document Number	Rev	
	FX6	3A	
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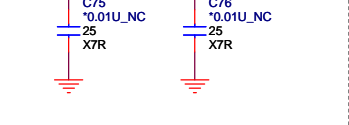
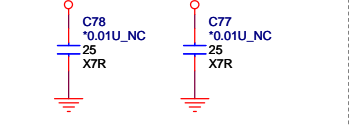
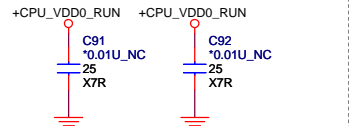
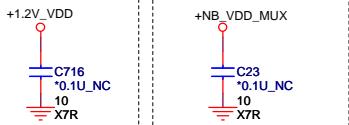
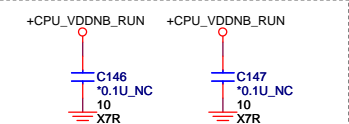
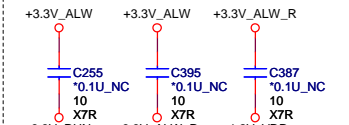
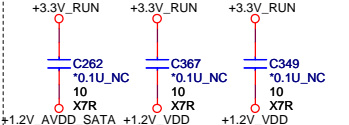
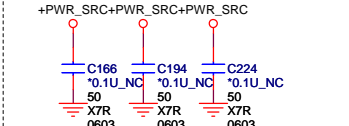
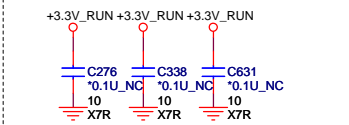
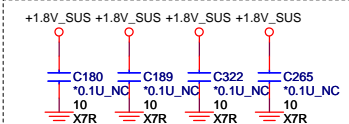
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Title: VGA_M82			
Size	Document Number FX6		Rev 3A
Date:	Tuesday, June 03, 2008		Sheet 55 of 70



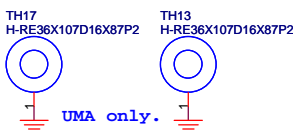




H-C315D
110P2-V4



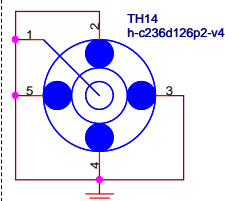
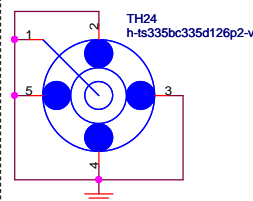
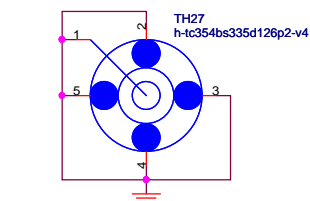
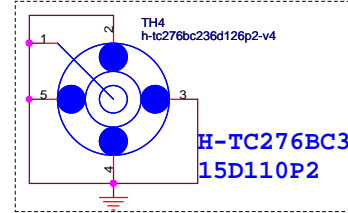
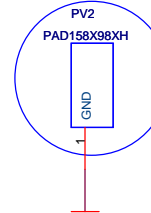
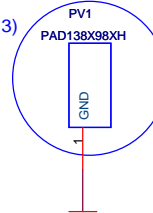
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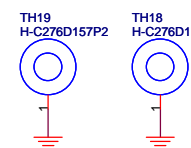
TH26
H-O126X158D126X158N



(13)

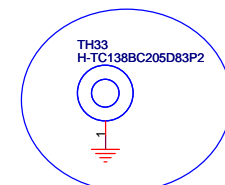
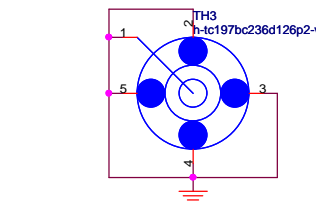
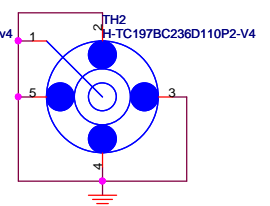
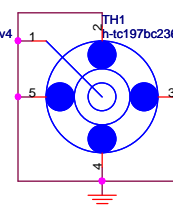
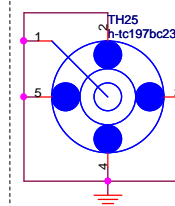
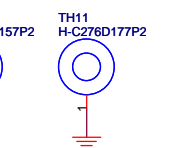


H-C276D157P2

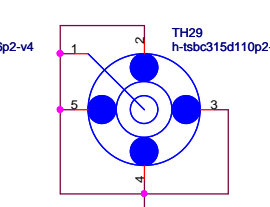
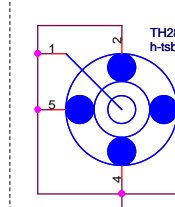
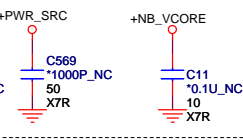
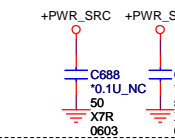
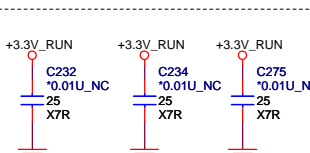
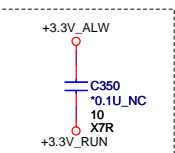


CPU TH

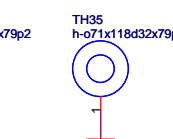
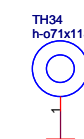
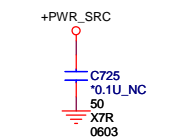
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h-o71x118d32x79p2



Title		
SCREL HOLE		
Size	Document Number	Rev
B	FX6	3A
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Item	Page#	Date	T	Issue Description	Solution Description	Rev	
				X00-1			
4	1	25	8/13/2007	EE	CLK_NB_14MB need resistor to a voltage divider. RS780 voltage level is +1.1V.	Chagne R607 from 33 ohm to 158/F, added R637 90.9/F, depop R608 10k for RS780.	X00-1
	2	4	8/13/2007	EE	Remove R516 0 ohm reserved resistor for MEMVREF. FX6/GX3 use 1.8V/2	Remove R516 0 ohm.	X00-1
	3	5,12	8/13/2007	EE	CPU_LDT_REQ#R should pull up to +1.8V_SUS.	POP R38 and Depop R415.	X00-1
	4	8,51	8/13/2007	EE	Connect STRP_DATA to VCORE PWM of NB for Power play.	Connect STRP_DATA from U23.B10 to PQ1.2.	X00-1
	5	13	8/13/2007	EE	IDE_RST#/F_RST#/IMC_GPO3 defaults to output driven low.	Remove R720 20k.	X00-1
	6	14	8/13/2007	EE	GP16,GP17 for ROM sel. Hepburn connect to EC spi rom. For SB, EC is on LPC bus.	Depop R430 and pop R420. For LPC.	X00-1
	7	14	8/13/2007	EE	ATI recommend that AVDD should tie to +3.3V_S5 power rail.	Chagne L46 from +3.3V_SUS to +3.3V_ALW.	X00-1
	8	14	8/13/2007	EE	ATI recommend that AZ_RST#, LPCCLK0, LPCCLK1 should pull up to +3.3V_S5 with a 10-k.	Chagne R378,R396,R408 from +3.3V_SUS to +3.3V_ALW.	X00-1
	9	8	8/13/2007	EE	S1G2 didn't use DDR_CS2_DIMMA/B# pin.	Remove DDR_CS2_DIMMA/B# from CN5,CN6	X00-1
					Chagne from X00-1 to X00-2		
3	10	08	8/14/2007	EE	Follow ATI recommend.	Change Q59,Q20 from MMBT3904 to FDV301N and remove R54,R492.	X00-2
	11	5	8/14/2007	EE	Follow ATI recommend.	Modify VID table.	X00-2
	12	16	8/14/2007	EE	Remove single net DDR_CS3_DIMMA/B#	Remove single net CN5.120,CN6.120	X00-2
	13	5	8/14/2007	EE	Change the CPU_PWRGD,LDT_STOP#, LDT_RST# from +1.8V_RUN to +1.8V_SUS.	Pull-up R193,R180,R184 from +1.8V_RUN to +1.8V_SUS(VDDIO).	X00-2
	14	5	8/14/2007	EE	Follow ATI recommend.CPU pin C2 need pull-down with 0 ohm.	Pop R536 0 ohm.	X00-2
	15	5	8/14/2007	EE	To save the space. There is no need to have these resister in Griffin system.	Remove R556,R169,R161,R554,R553,R555,R172,R191,R165,R168,R196,R205	X00-2
	16	5	8/14/2007	EE	Follow ATI.The HDT we have (you have) right now is Purple Possum system. It's 1.8V level design.	Pop R213 0 ohm and depop R212,Q35,R216.	X00-2
	17	5,53	8/14/2007	EE	CPU_PWRGD_SVID_REG should be level shifted to 3.3V for the ISL6265. Vih(min) is 2V.	Added Q76,R161.	X00-2
	18	5	8/14/2007	EE	Diode D7 blocks a low input to the CPU MEMHOT_L so the circuit would not work as drawn	Remove D7 and reserved R159 680 ohm for DDRII thermal IC in the future.	X00-2
2	19	19	8/14/2007	EE	HDMI strap is on Hsync.Add 10k-ohm PU (to 3.3V) on VGAHSYNC before buffer U6. Discrete only.	Pull up R191 10k ohm to +3.3V_RUN at VGASYNC	X00-2
	20	8,28	8/14/2007	EE	DDC3 is 5V tolerance. There is no need to add level shifters, Discrete only.	Remove R18,R19,R22,R30,Q12,Q18. Remove off page HDMI_SCL,HDMI_SDA.Add TP on U23.A8	X00-2
	21	39	8/14/2007	EE	For LPC connect to WPAN socket: Reserve 0ohm, and NC when PD.	Added R720,R763~R766 0 ohm for LPC signals.	X00-2
					Chagne from X00-2 to X00-3		
	22	29	8/15/2007	EE	Reserve the caps for any noise coupling issue happening.	Depop C338 and close Q37. Added C920 and close EMC1423.	X00-3
	23	29	8/15/2007	EE	Added Q77 2N7002 isolation circuit.	Added Q77 instead R406 ohm and change Q42 from +3.3V_SUS to +3.3V_RUN.	X00-3
	24						X00-3
	25						X00-3
	26	49	8/15/2007	P	FAE Suggetion for OCP setting	Change PR97 from 7.15K to 8.45K	X00-3
1	27	52	8/15/2007	P	Charge pump from +5V LDO, might cause high ripple voltage	Add P112 to reduce ripple voltage	X00-3
	28	52	8/15/2007	P	PR219 no need such hige rating component	Change PR219 from 0805 to 0603 and remove one	X00-3
PROJECT : Hepburn				DOC. NO. : 204		REV: X00	
APPROVED BY : Cory Lin				CHECKED BY: Cory Lin		DRAWN BY : Leo Tseng	
				DATE : Aug. 13 , 2007		SHEET 1 OF 11	
						 QUANTA COMPUTER	

Item	Page#	Date	T	Issue Description	Solution Description	Rev
29	52	8/15/2007	P	PC474 should populated for filter	Populate PC474	X00-3
30	52	8/15/2007	P	Reserve feedback circuit for testing	Add PR169 and PR218	X00-3
31	28	8/15/2007	EE	No need to implement shunt resistors for HDMI on M82S Discrete only.	Remove R159,R160,R163,R164 180 ohm.	X00-3
32	36	8/15/2007	EE	Follow vendor review. Added RC to include more different memory card.	Pop C860 270pF and added C921 0.01u, R456 150k.	X00-3
33	19,27	8/15/2007	EE	Follow M82-S reference schematic. Discrete only.	There is double PU for CRT DDC.Remove R522,R519 2.2k and change R520,R486,R521,R485 to 2.2k.	X00-3
				Chagne from X00-3 to X00-4		
34	42	8/16/2007	P	Load switch voltage drop is out of spec.	Change PQ13 from SI4800BDY to SI4856BDY	X00-4
35	42	8/16/2007	P	Load switch voltage drop is out of spec.	Change PQ29 from SI4800BDY to SI4336DY	X00-4
36	42	8/16/2007	P	Load switch voltage drop is out of spec.	Change PQ20 from SI4800BDY to SI4336DY	X00-4
37	5,29	8/16/2007	EE	Follow SMSC feedback.	Change C341 from 220p to 2200p and depop C212	X00-4
38	15	8/16/2007	EE	Follow ATI SB700 checklist.	Change C518,C519,C529 to 1uF, C524 to 22uF.	X00-4
39	15	8/16/2007	EE	Follow ATI SB700 checklist.	Change C496,C494,C495,C489 to 2.2uF.	X00-4
				Chagne from X00-4 to X00-5		
40	19	8/17/2007	EE	Move CLK_VGA_27M_SS to GPIO16 and reserved it for spread spectrum. Discrete only.	Reserved R196 0 ohm for EXT CLK GEN.	X00-5
41	29,43,44	8/17/2007	EE	Added ESD diode.	Added D35,D36,D37,D38	X00-5
42	38	8/17/2007	EE	Follow ATI SB700 checklist.	Change C96,C208 from 0.01u to 0.1u to meet SB700 checklist.	X00-5
				Chagne from X00-5 to X00-6		
43	8	8/20/2007	EE	Change VGAH(V)SYNC to INT_VGAH(V)SYNC from PU to PD for disable side prot memry. Discrete only.	Depop R497 and pop R500.	X00-6
44	25	8/20/2007	EE	It's no need to reserve 49.9 ohm and change R243,R235 from 47.5 to 0 ohm, depop R236 261/F.	Remove 49.9 ohm, change R243,R235 from 47.5 to 0 ohm and depop R236.	X00-6
45	25	8/20/2007	EE	Follow FAE feedback. Added Decoupling caps for U16's VDDIO.	Added Decoupling caps C685,C924~C930 and L93 for U16's VDDIO.	X00-6
46	12,20	8/20/2007	EE	Follow ATI FAE recommend. Set GPIO to turn on M82 +3.3V_DELAY. Discrete only.	Connect GFX_RUN_ON from SB700 pin AC6 to R513.	X00-6
47	12,14,18	8/20/2007	EE	Follow ATI FAE recommend to change the M82 reset signal for power express. Discrete only.	Added R458,R457,D39,D40,R205 for power express.	X00-6
48	14	8/20/2007	EE	Follow ATI FAE recommend.	Change R421,R429 from 10k to 2.2k.	X00-6
49	34	8/20/2007	EE	Follow BCM FAE recommend to remove external RC termination.	Remove (R690~R697 and C794~C797)	X00-6
50	33	8/20/2007	EE	Follow BCM recommend to add the required grounding for all the package signals and powertermination.	Add U29 pin 69 thermal GND pad.	X00-6
				Chagne from X00-6 to X00-7		
51	42	8/21/2007	EE	Follow Card reader vendor recommend to add PU resistor for IRQ_SERIRQ.	Add R267 10K ohm to pull-up +3.3V_RUN.	X00-7
52	41	8/21/2007	EE	There is no +3.3V_RTC_LDO power rail.	Change the +3.3V_RTC_LDO to +3.3V_ALW.	X00-7
53	21	8/21/2007	EE	Added +1.8V_GFX power rail for M82-S power express Discrete only.	Change the M82-S +1.8V_RUN to +1.8V_GFX and added +1.8V_GFX power switch.	X00-7
54	51	8/21/2007	P	Connect thermal pad to AGND	Add pin15 to AGND	X00-7
55	52	8/21/2007	P	Preserve component for MAX8778	Add PC115	X00-7
56	54	8/21/2007	P	Connect thermal pad to AGND	Add pin15 to AGND	X00-7
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57	55	8/21/2007	P	Change feedback resistor for 1.1V output	Change PR66 to 63.4K	X00-7
58	55	8/21/2007	P	Change feedback resistor for +1.1V_GFX_PCIE output	Change PR68 to 4.53K	X00-7
				Chagne from X00-7 to X00-8		
59	12,35	8/22/2007	EE	Change the PCI_PIRQD to PCI_PIRQB. ATI must use INTH#/GPIO36 to control M82-S reset signal.	Change the PCI_PIRQD to PCI_PIRQB and move to U31.AC4	X00-8
60	12	8/22/2007	EE	ATI use INTH#/GPIO36 (PE_GPIO0) to control M82-S reset signal.	Added PE_GPIO0 on U31.AE3 to control M82-S reset.	X00-8
61	48	8/22/2007	P	Pin define is wrong.	Change JABT1 pin define	X00-8
62	48	8/22/2007	P	Remove AC_OFF function	Remove PQ24	X00-8
63	9	8/23/2007	EE	Remove resistor for RX780.	Remove R490,R42,R84,R32,R63,R112,R119,R131 for RX780.	X00-8
64	22	8/23/2007	EE	Added level shift on M82-S thermal IC SMBUS2. Discrete only.	Added Q88,Q87 and remove R144,R137 0 ohm.	X00-8
65	34	8/23/2007	EE	Follow FM6 to modify the +3.3V_LAN power source form +3.3V_ALW to +3.3V_SUS.	Depop +3.3V_ALW to +3.3V_LAN switch circuit and added R767 to connect +3.3V_SUS to +3.3V_LAN.	X00-8
66	55	8/23/2007	EE	We don't use RUNPWROK and use GFX_RUN_ON to turn on GFX power.	Remove PR169.	X00-8
67	12	8/23/2007	EE	Follow ATI checklist. Reserved J13 for Rubuto.	Added J13 for Rubuto system.	X00-8
68	34	8/23/2007	EE	Follow Dell. Change the LED signals.	LINKLED connect to G_LED.SPD100LED connect to amber LED.	X00-8
				Chagne from X00-8 to X00-9		
69	9	8/24/2007	EE	Check the CLK GEN vendor (RT&CLG). They don't have PA_RS7X0A1 issue.	Remove R29,R33,R37,R34 and connect to GPP_SB_REFCLK directly from CLK GEN SB_SRC CLK.	X00-9
70	26	8/24/2007	EE	Added OR gate to support backlight from EC and NB.	Added U225,C932 and pop R464.	X00-9
71	45	8/24/2007	EE	Added AND gate in system reset circuit.	Remove R204,R209 and added U226,U227.	X00-9
72	31,32	8/24/2007	EE	Change the audio to IDT STAC9228/92HD73C.	Change the audio to IDT STAC9228/92HD73C.	X00-9
73	25	8/24/2007	EE	Follow RS780 check list to change the ferrite bead for CLK GEN power.	Change the L34 ,L93 and added L107,L108 to FBM-11-160808-601A10T	X00-9
74	11	8/24/2007	EE	Follow RS780 check list.	Added C997,C998 1U and change L15 from 4.7U to 1U.	X00-9
				Chagne from X00-9 to X00-10		
75	22,26	8/28/2007	EE	Added reduce WWAN interference solution.	Added C1001-C1008, R835,R836.	X00-10
76	42,43	8/28/2007	EE	Chagne MEDIA_INT to active low. MEDIA_INT# need pull-up +3.3V_ALW.	Move R217 to page 43, pull-up to +3.3V_ALW. Added RC to MEDIA_INT#.	X00-10
77	44	8/28/2007	EE	Chagne power switch and sniffer switch power rail.	Chagne R461,R21 from +RTC_CELL to +3.3V_ALW.	X00-10
78	42,53	8/28/2007	EE	Chagne CPU_VCORE_PWRGD pull up power rail.	Chagne PR35 from +3.3V_ALW to +3.3V_SUS and depop R574.	X00-10
79	43	8/28/2007	EE	Added the NUM, CAP low active circuit and swap keyboard signals.	Added CP7 and Q80,Q82,Q81,Q83,R834,R832.	X00-10
80	39	8/28/2007	EE	Depop debug board's 0 ohm.	Depop debug board's 0 ohm R322,R685,R720,R763,R764,R765,R766	X00-10
81	30	8/28/2007	EE	ODD SATA is not need +3.3V_RUN. Remove +3.3V_RUN decoup caps for ODD SATA.	Remove R745,R747,R307,R744,R313.	X00-10
82	46	8/28/2007	P	USB Charger Function	Add +5V_ALW to +5V_SUS Load Switch for USB Charger	X00-10
83	52	8/28/2007	P	USB Charger Function	Change +5V_ALW to +5V_ALW2	X00-10
84	52	8/28/2007	P	USB Charger Function	Change +5V_SUS to +5V_ALW	X00-10
85	52	8/28/2007	P	USB Charger Function	Remove PR213 and PD1	X00-10

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86	52	8/28/2007	P	USB Charger Function	Change +3.3V_DL to +5V_DL	X00-10
87	51	8/28/2007	P	FAE Suggest 237K for 300KHz frequency	Change from 178K to 237K	X00-10
88	54	8/28/2007	P	FAE Suggest 237K for 300KHz frequency	Change from 178K to 237K	X00-10
89	49	8/28/2008	P	FAE Suggest connect to GND	Change to connect to GND	X00-10
90	49	8/28/2008	EE	Follow AMD recomment. Added buffer work around circuit to NB_PWRGD.	Added U234 buffer to seperate NB_PWRGD and WD_PWRGD.	X00-10
				Chagne from X00-10 to X00-11		
91	25	8/29/2008	EE	Added MINI3CLK_REQ#,EXPRESSCARD_REQ# pull-up resistor.	Added R837,R859 10k pull up to +3.3V_RUN.	X00-11
92	9	8/29/2008	EE	pop R495 and remove PANEL_BKEN from RS7800	pop R495 0 ohm and remove R806.	X00-11
93	28,44	8/29/2008	EE	Add ESD, Choke for Biometric and HDMI.	Add ESD3 for Biometric and L109-L112 for HDMI.	X00-11
94	24	8/29/2008	EE	Follow AMD recomment. Change the voltage level for hybrid IC SEL pin.	Change R89 from 0 ohm to 8.2k ohm.	X00-11
95	10	8/30/2008	EE	Add work around TPS72501 to create 1.35V to RS780 VDDHTTX power rail. RS780 Rev.A11 only.	Used TPS72501 to create +1.35V_HT_VCC and added L113 for option.	X00-11
96	9	8/30/2008	EE	Added PD resistor 2.7k for INT_EN_LCDVDD.	Added R863 2.7k for INT_EN_LCDVDD.	X00-11
97	10	8/30/2008	EE	Follow ATI checklist. Added L114 to reduce noise for VDDPCIE.	Added L114 to VDD_PCIE.	X00-11
98	46	8/30/2007	P	For more suitable RDSON	Change to SI4800BDY	X00-11
99	48	8/30/2007	P	Footprint is not correct	Change to new footprint "BAT-200045MR009H577ZR-9P-R-V"	X00-11
100	49	8/30/2007	P	MPL104S-0R9 is not PSL	Change to MPC1040LR88	X00-11
101	52	8/30/2007	P	Reserve GPIO for USB Charger	Add 5V_ALW_ON GPIO for USB charger enable	X00-11
102	52	8/30/2007	P	FAE suggest connect to +3.3V_DL	Connect to +3.3V_DL	X00-11
103	52	8/30/2007	P	For Uni material	Change to 0.1u/0603	X00-11
104	53	8/30/2007	P	MPL73-3R3 is not PSL	Change to MPLC0730L3R3	X00-11
105	53	8/30/2007	P	FAE Suggest PR43=18K, PR42=100K	Change to PR43=18K, PR42=100K	X00-11
106	53	8/30/2007	P	FAE Suggest PR198=16.2K, PR205=4.02K	Change to PR198=16.2K, PR205=4.02K	X00-11
107	53	8/30/2007	P	FAE Suggest PR199=16.2K, PR200=4.02K	Change to PR199=16.2K, PR200=4.02K	X00-11
108	54	8/30/2007	P	MPL73-4R7 is not PSL	Change to MPLC0730L4R7	X00-11
109	54	8/30/2007	P	For High=1.0, Low=0.9 Output	Change PR207 to 20K/F	X00-11
110	55	8/30/2007	P	For High=1.0, Low=0.9 Output	Change PR64 to 69.8K/F	X00-11
111	56	8/30/2007	P	For High=1.0, Low=0.9 Output	Change PR66 to 22.6K/F	X00-11
				Chagne from X00-11 to X00-12		
112	32	8/31/2007	EE	Follow ME feedback. Used MIC connector in MB side.	Pop J14 and remove M1	X00-12
113	19,20	8/31/2007	EE	Follow ATI FAE. Reserved GFX thermal protect function.	Added U241,Q98,Q99,R870,R871.R872	X00-12
114	53	9/1/2007	P	FAE Suggest to remove sense resistor for saving space	Remove PR179, PR180	X00-12
115	53	9/1/2007	P	FAE Suggest to remove sense resistor for saving space	Remove PR194, PR195	X00-12
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116	55	9/01/2008	P	Change to hight rating mosfet for 9.4A	Change to FDS8880_NL	
117	55	9/01/2008	P	Change to hight rating mosfet for 9.4A	Change to FDS6676AS_NL	
118	55	9/01/2008	P	Change to hight rating mosfet for 9.4A	Change to SIL104R-1R0	
119	47	9/01/2008	P	Cancel this function. It's no use.	Remove PR74, PQ15	
120	29	9/01/2008	EE	Follow FAE feedback. Pull up resistor to +3.3V_SUS.	Added R877 10k ohm to pull up +3.3V_SUS.	X00-12
121	36	9/01/2008	EE	Follow FAE feedback. Added C1032 270p_NC to SD_CD#	Added C1032 270p_NC to CON5 pin 2 SD_CD#.	X00-12
122	15	9/01/2008	EE	Follow AMD feedback. Change SB700 VDD power rail from +1.2V_RUN to +1.2V_ALW_SUS.	Added L90 and connect to +1.2V_ALW_SUS. Depop L39.	X00-12
123	24	9/01/2008	EE	Follow AMD feedback. Change R89 from 0 ohm to 8.2k ohm.	Change R89 from 0 ohm to 8.2k ohm.	X00-12
124	26	9/01/2008	EE	Reserved caps for reduce SMBUS1 overshoot and under shoot.	Reserved C1011,C1012 47p in J1 pin5,6	X00-12
125	52	9/03/2008	P	Reserved for MAX8778	Add PR114	X00-12
126	55	9/03/2008	P	Reserved snubber	Add PR245, PC211	X00-12
127	42	9/03/2008	EE	ITE 8512 FAE concern pin 126,pin 23,pin 4,pin 15 have leakage .	Added D43~D46 to U13 pin 126, pin 23, pin 4, pin 15.	X00-12
128	5	9/03/2008	EE	Follow AMD feedback. Added 2 * MOSFET for CPU_PWRGD_SVID_REG level shift.	Added Q100,R881and modify Q76 to gate by CPU_PWRGD.	X00-12
				Chagne from X00-12 to X00-13		X00-12
129	49,51,54	9/04/2008	P	Dell suggest to add 0.1u cap near IC feedback pin to reduce feedback noise.	Add 0.1u cap	X00-13
130	51	9/04/2008	P	FAE suggest to add PR460,PC451 and PQ115 for voltage shift function.	Aadd PR460,PC451 and PQ115 for voltage shift function.	X00-13
131	19	9/04/2008	EE	Follow ATI feedback.	Reserved R889 1M for Y2 27Mhz.	X00-13
132	42	9/04/2008	EE	Added D47	Added D47 to connect WRST# and THERM_STP#	X00-13
133	33	9/04/2008	EE	Reserved BCM5784M SUPER_IDDQ circuit.	Reserved R888 20k ohm.	X00-13
134	9,27	9/04/2008	EE	Add RS780 CRT I2C function.	Connect U13 pin E8,F8 to CRT DDC bus.	X00-13
135	9,28	9/04/2008	EE	Add RS780 HDMI I2C function.	Connect U13 pin A8,B8 to HDMI DDC bus and Added level shift(R886,R887,Q101,Q102)	X00-13
				Chagne from X00-13 to X00-14		
136	31	9/05/2008	EE	Added 4 * 0 ohm for EMI.	Added R898~R901 to JSPK1.	X00-14
137	55	9/05/2008	EE	Footprint is different with PL9 sepc.	Change PL9 footprint to SIL104.	X00-14
138	24	9/05/2008	EE	ATI has update power express circuit.	Added R890~R897and depop Q3~Q10.	X00-14
139	13,39	9/05/2008	EE	Added SB_USBP8 to WLAN.	Added L115, R902, R903.	X00-14
				Chagne from X00-14 to X00-15		X00-15
141	43	9/06/2008	EE	Added KB BACKLITE power switch circuit.	Added Q104,Q103,C1033,C1034,R190,R907,R908,R909 to option +KB_LED power source.	X00-15
142	43	9/06/2008	EE	Added TP power rail and change LID_SW# power rail	Added C385 and PU to +3.3V_SUS to JP2.5. Change R455 to +3.3V_ALW.	X00-15
				Chagne from X00-15 to X00-16		
143	9	9/11/2008	EE	There is on need pull-up resistor to work around for RS780 A11.	Depop R416	X00-16
144	44	9/12/2008	EE	There is not work in DC IN LED for SSI build.	Depop Q16, Q17, R44, R45	X00-16

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CHECKED BY: Cory Lin

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145	9	9/14/2007	EE	Follow ATI FAE feedback. Change the RS780 strap pin.	Depop R419 and pop R420.	X00-16
				Chagne from X00-16 to X01-1		
1	9	10/01/2007	EE	Follow ATI FAE feedback. Don't need LDT_STOP#, CPU_LDT_REQ# level shift.	Depop the level shift Q52,Q3,R341,R39 and added R637, R638 0 ohm.	X01-1
2	9	10/01/2007	EE	Follow ATI FAE feedback. Change the RS780 debug strap pin.	Added R639 3k ohm to PU +3.3V_RUN and depop the R349.	X01-1
3	12	10/26/2007	EE	Follow AMD SCL.	Depop R694 1M ohm.	X01-1
P1	52	10/30/2007	P	ALW_PWRGD_3V_5V is dummy net	Remove PR178,PR182 and change connect to +3.3V_ALW	X01-1
P2	51	10/30/2007	P	NB_VCORE will OVP when voltage switch	Follow FAE suggestion to put PR178 and PR182	X01-1
P3	47,48	10/30/2007	P	+5V_ALW issue when USB charger disabled in S5	Change +5V_ALW to +5V_ALW2 for below terminal PU6.8, PR115,PR22, PD4.1, PD5.1	X01-1
P4	47	10/30/2007	P	To solve EE noise made by charger	Change charger output Cap 10U/25V from X6S to X5R CAP (PN: CH6104K9207)	X01-1
P5	51	10/30/2007	P	Change capacitor to resistor for reserve pull low	Change PC11 to PR214	X01-1
P6	54	10/30/2007	P	1.2V_ALW_SUS_ON is floating	Add a resistor PR215 to pull low	X01-1
P7	47,51,52	10/30/2007	P	SI4810 EOL Issue	Change PQ40,PQ2,PQ22,PQ26 to SI4812	X01-1
P8	51,54	10/30/2007	P	To reduce Vo jitter issue	Change PC57 and PC86 to 220u/2.5V/ESR15	X01-1
4	10	10/31/2007	EE	RS780M change form A11 to A12 and don't need work around.	Pop L54 and Depop L55,C488,U20,R381,R382,C491.	X01-1
5	13,37,42	10/31/2007	EE	Added Express card power enable on SB700. It's for Express card hot plug.	Change U30.B8 from USB_OC5# to EXPRCRD_PWREN# and connect to CN2.	X01-1
6	28	10/31/2007	EE	Follow ANT HDMI detect circuit.	Added Q80, and remove R336,D19	X01-1
7	32	10/31/2007	EE	Added +3.6V_CAMERA Camera power circuit	Added U43,C741,C743,C742,R640,R642.Remove C527. Modify JCAMERA1 pin define and L58 power rail.	X01-1
8	38	10/31/2007	EE	Added USB charge circuit for leakage.	Added Q81,R643,U44,U45.	X01-1
9	42	10/31/2007	EE	Swap U5.31 NUM_LED# and U9.98 KB_BACKLITE_EN	Swap U5.31 NUM_LED# and U5.98 KB_BACKLITE_EN	X01-1
10	44	10/31/2007	EE	Depop SNIFFER_YELLOW LED circuit. and Swap WIRELESS_ON/OFF#, SNIFFER_PWR_SW# circuit.	Depop R377,Q55,Q54,R371 and Swap R376 SNIFFER_PWR_SW#, R313 WIRELESS_ON/OFF# signals	X01-1
11	43	10/31/2007	EE	Change KB_LED pwoer ciruit.	Pop R507, Add Q82 and Depop R513,R512,Q71,Q70,C589,C579,R505 and modify J4 pin define.	X01-1
12	9,45	10/31/2007	EE	Depop SB700 A11 WD_PWRGD work around circuit.	Depop U11,C222,R186 and pop R186,R344	X01-1
13	42	11/01/2007	EE	Change GPIO and remove SNIFFER_YELLOW function.	Move 5V_ALW_ON to U5.83, Move NUM_LED# to U5.88 and remove R377,Q55,Q54,R371	X01-1
				Chagne from X01-1 to X01-2		
14	5,12	11/01/2007	EE	+5V_ALW issue when USB charger disabled in S5	Change R87,R306 from +5V_ALW to +5V_ALW2.	X01-2
15	33,34	11/02/2007	EE	Change BCM5787M to BCM5784M.	Change BCM5787M to BCM5784M.	X01-2
16	31	11/02/2007	EE	Change STAC9228 to 92HD73C.	Change STAC9228 to 92HD73C.	X01-2
17	14	11/05/2007	EE	Follow ATI SCL and feedback.	Added R644 0 ohm connect U30.C6 TEMP_COMM to GND.	X01-2
18	13,39	11/05/2007	EE	Change WLAN from USB port 8 to USB port 4.	Change WLAN from SB_USBP8+/- to SB_USBP4+/- and Move to U30.B12,U30.A12.	X01-2
19	38	11/05/2007	EE	Co-lay USB Q-switch and 0 ohm	Reserved R645~R648 0 ohm with U44 pin 2,3,5,6,U45 pin 2,3,5,6.	X01-2
P1	52	10/30/2007	P	ALW_PWRGD_3V_5V is dummy net	Remove PR178,PR182 and change connect to +3.3V_ALW	X01-2
P2	51	10/30/2007	P	NB_VCORE will OVP when voltage switch	Follow FAE suggestion to put PR178 and PR182	X01-2
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P3	47,48	10/30/2007	P	+5V_ALW issue when USB charger disabled in S5	Change +5V_ALW to +5V_ALW2 for below terminal PU6.8, PR115,PR22, PD4.1, PD5.1	X01-2
P4	47	10/30/2007	P	To solve EE noise made by charger	Change charger output Cap 10U/25V from X6S to X5R CAP (PN: CH6104K9207)	X01-2
P5	51	10/30/2007	P	Change capacitor to resistor for reserve pull low	Change PC11 to PR214	X01-2
P6	54	10/30/2007	P	1.2V_ALW_SUS_ON is floating	Add a resistor PR215 to pull low	X01-2
P7	47,51,52	10/30/2007	P	SI4810 EOL Issue	Change PQ40,PQ2,PQ22,PQ26 to SI4812	X01-2
P8	51,54	10/30/2007	P	To reduce Vo jitter issue	Change PC57 and PC86 to 220u/2.5V/ESR15	X01-2
P9	46	11/05/2007	P	Modify +5V_SUS load switch	Remove PQ12	X01-2
P10	53	11/05/2007	P	FAE suggest to reserve	Add PR241	X01-2
P11	54	11/05/2007	P	Modify current limit value	Change PR228 from 10K to 5.9K	X01-2
P12	49,51,53,54,55	11/05/2007	P	To solve power good glitch issue	Connect IC power to +5V_ALW2	X01-2
P13	49	11/05/2007	P	Set tracking discharge mode	PR206 populate and PR208 NC	X01-2
P14	52	11/05/2007	P	5V_ALW_ON pull low at initial state	Add PR218	X01-2
P15	53	11/05/2007	P	CPU_VCORE_ENABLE pull low at initial state	Add PR219	X01-2
20	42,44,48	11/06/2007	EE	Remove DC IN LED circuit and change signal name DCIN_DETECT_LED# to CHIPSET_ID1.	Remove R37,Q10,Q9,R69 and change U5.99 signal name DCIN_DETECT_LED# to CHIPSET_ID1.	X01-2
P16	51,54	11/06/2007	P	For space saving.	Remove PC2,PC81.	X01-2
21	42	11/07/2007	EE	Add BID1 to EC pin98	Connect R130,R131 to U5.98	X01-2
22	25,42	11/07/2007	EE	Remove double pull-up resistor.	Remove R107,RP2,R455	X01-2
				Chagne from X01-2 to X01-3		
23	5	11/09/2007	EE	Solve glitch from CPU_PWRGD.	Added C744 0.1uF on CPU_PWRGD.	X01-3
24	14,42	11/09/2007	EE	Solve S5 leakage.	Connect L38 from +3.3V_ALW to +3.3V_SUS and remove R92 for SIO_SLP_S5#.	X01-3
P17	49,51,54	11/12/2007	P	Reserve for solving glitch issue caused by IC power rail	Add PR220,PR221,PR222,PR223,PR224	X01-3
P18	51	11/12/2007	P	Follow AMD FAE suggest +NB_VCORE dynamic voltage design	Remove PQ7,PC13,PR19,PR12	X01-3
P19	54	11/12/2007	P	To solve jitter issue	Change PL2 from 4R7 to 3R3	X01-3
25	43	11/14/2007	EE	Follow ANT reference to solve S3 leakage.	Change R389,R99,R97,R90 pull-up from +1.8V_SUS to +1.8V_RUN.	X01-3
26	12	11/15/2007	EE	Solve CPU_PWRGD voltage too low(+1.5V).	Change Q36 from MMBT3904 to FDV301N.	X01-3
27	42	11/15/2007	EE	Check with power team and EC. The charge IC INP pin can be read with EC ADC function.	Pop R86 0 ohm and depop R91 0 ohm.	X01-3
28	14,33,36,42	11/15/2007	EE	Follow XTAL vendor feedback to change the XTAL caps.	Change C139, C149 to 18pF. C394 to 27pF. C556 to 22pF, C658, C659 to 12pF	X01-3
29	43	11/15/2007	EE	Follow Dell recommend.	Change R507 0 ohm to FS3.	X01-3
30	31,32	11/16/2007	EE	Follow IDT recommend to change caps for batter Audio Precision.	Change C730, C724, C622, C620 from 1uF to 2.2uF.	X01-3
31	5,12	11/16/2007	EE	Follow ANT 3.2 reference schematic to remove CPU_PROCHOT# level shift.	Remove R441, R436, Q65.	X01-3
				Chagne from X01-3 to X01-4		
32	9	11/19/2007	EE	Update RS780M symbol.	Update U16 symbol.	X01-4

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CHECKED BY: Cory Lin


DRAWN BY : Leo Tseng


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P20	46	11/19/2007	P	Reduce RUN/SUS PW switch circuit.	Remove PR(89,93,197,200,170,168,68,66) and change PQ(34,51,49,20) to 2N7002W-7-F.	X01-4
P21	46	11/19/2007	P	Reduce RUN/SUS PW switch circuit.	PC58,PC32,PC43,PC51,PC30,PC36,PC175 from 10U/1206 to 0.1U/0603	X01-4
33	44	11/19/2007	EE	Sniffer should be during S5.Dell define our Sniffer switch need to stay 'ON' after the WiFi can be enable.	change R313 to +3.3V_ALW.	X01-4
34	14	11/19/2007	EE	Follow AMD SB700 design guideline to add series resistor.	Add R649, R650 4.99 ohm at U39 AD13,AE13 SATA_TX3+/- for ESATA signals.	X01-4
35	14	11/20/2007	EE	Depop Q-switch function on PT build.	Depop Q81,R643,U44,U45 and pop R645~R648.	X01-4
P22	47	11/20/2007	P	UL schemaitc are going to be replaced by EC control	UL schemaitc components are NC	X01-4
P23	49	11/20/2007	P	Reduce Jitter	Change PC183 and PC184 from 330u/ESR15 to 220u/ESR25	X01-4
P24	52	11/20/2007	P	PC168 is no use for schematic	Remove PC168	X01-4
P25	53	11/20/2007	P	To reduce input ripple	Add PC190 and PC191	X01-4
P26	47,48	11/20/2007	P	2nd Source suggest to change	Change PD8 to RB500V-40 , PQ4 to FDV301N	X01-4
36	42	11/21/2007	EE	Follow ITE feedback to reserve caps for ITE8512JX.	Add C745, R651 to U9 pin 12.	X01-4
37	38	11/21/2007	EE	Change USB Q-switch power rail from +3.3V_RUN to +3.3V_SUS.	Change U44 pin 8, U45 pin 8 from +3.3V_RUN to +3.3V_SUS, Q81 pin2 from RUN_ON to SUS_ON.	X01-4
38	33,34	11/21/2007	EE	Modify LAN 1000 LED circuit to solve BCM5784M LED issue.	Add D36,R774 to solve BCM5784M 1000 LED issue.	X01-4
39	28	11/22/2007	EE	Change HDMI connector symbol.	Change CN3 connector symbol.	X01-4
40	28	11/22/2007	EE	Remove these 20K ohm resistors because it is for desktop design or codec internal headphone amplifier.	Depop R519, R521, R532, and R547.	X01-4
41	38	11/22/2007	EE	For EMI solution to pop choke.	Pop L19,L20 and depop R78, R83,R85,R88.	X01-4
42	50	11/23/2007	EE	Base on RS780M T13 timing. +1.8V_RUN rise need before then +1.1V_RUN.	Change PR62 from 0 ohm to 200k ohm and depop PC41 from 0.01u to 0.1u.	X01-4
P27	53	11/24/2007	P	EMI Solution	Add PC168,PC192,PC193,PC197,PC198,PC199,PC194,PC195,PC196	X01-4
P28	48	11/24/2007	P	For ESD protect	EMI Suggestion PD6 populate	X01-4
43	25	11/23/2007	EE	EMI Solution	EMI Suggestion C565, C575 populate	X01-4
44	12	11/23/2007	EE	EMI Solution	EMI Suggestion C292 populate	X01-4
45	32	11/23/2007	EE	EMI Solution	EMI Suggestion C573,C584,C595,C603 change form 220pF to 470pF.	X01-4
46	32	11/23/2007	EE	IDT had found out the resonance on portA and suggested change 220pF to 47pF for EMI.	Change C621, C609 from 220pF to 47pF.	X01-4
				Chagne from X01-4 to X01-5		
47	41	11/26/2007	EE	BT1 connector pin define is different before.	Change BT1 pin 2 to GND, pin 1 to +RTC.	X01-5
48	42	11/26/2007	EE	Sniffer power switch needs to wake up EC, when battery only. So it needs to use WUI pin.	Swap U5.108 SNIFFER_PWR_SW# and U5.35 WIRELESS_ON/OFF#	X01-5
49	36	11/26/2007	EE	EMI Solution	Add C758~C760 27pF for EMI solution.	X01-5
P29	51	11/26/2007	P	FAE suggest to reserve RC to slow down voltage switch	add the R/C at PQ53 to slow down PQ53 switcher to against OVP, and remove R/C in front of PQ5	X01-5
P30	51,54	11/26/2007	P	Got more performance for jitter issue	Change PC97 and PC72 from 220u/2.5V/ESR15 to 220u/4V/ESR40	X01-5
50	32	11/26/2007	EE	Follow FAE suggest.	Change U9 pin 21~25 to NC.	X01-5
51	38	11/26/2007	EE	EMI Solution	Populate ESD3 for EMI suggest.	X01-5
52	5	11/26/2007	EE	Solve system shut down issue from CPU_THERMTRIP#.	Add Q83,Q84,R776,C761 and connect H_THERMTRIP# to 3V, 5V ALW circuit.	X01-5
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53	12	11/28/2007	EE	Follow ANT 3.2 schematic.	Depop R576, R574.	X01-5
54	33	11/28/2007	EE	Follow Broadcom FAE feedback. BCM5784M CLKREQ# can't work.	Pop R434 ohm and depop R431 4.7k ohm before CLKREQ can work.	X01-5
				Chagne from X01-5 to X02-1		
1	5	12/28/2007	EE	Follow AMD Griffin sighting Dec 18.pdf to reserve resistor for system hang or shut downboot issue.	Add R777,R778 and pop R121 300 ohm resistor for system hang or shut down issue.	X02-1
2	43	1/2/2008	EE	Change MMB pin 1 power source to 5V_ALW to fix LED flash issue when AC/Bat plug in.	Change JP1.1 from +5V_ALW2 to +5V_ALW.	X02-1
3	43	1/4/2008	EE	Change Num, Cap power rail to +5V_RUN to fix Num, Cap LED flash issue when AC/Bat plug in.	Change Q57-Q60, R380, R379 power rail to +5V_RUN.	X02-1
4	38	1/10/2008	EE	Fulfill Reliability team request.	Connect JUSB1.8 to USB_BACK_PWR.	X02-1
5	43	1/11/2008	EE	Avoid system can enter S3 mode but wake up fail problem.	Change the lid switch IC power source from 3.3V_SUS to 3.3V_ALW.	X02-1
6	32	1/11/2008	EE	Change L61 to 22 ohm. It will help DMIC_CLK_L performance.	Change L61 to from 0 ohm to 22 ohm.	X02-1
7	38	1/11/2008	EE	Remove USB charge function.	Remove R643, Q81, U44, U45, R645-R648.	X02-1
8	38	1/14/2008	EE	Follow AMD AN_SB700AB5. Added re-driver IC to increase signal stress for ESATA.	Remove R649,R650 4.99 ohm. Added U50 3211B,R769-R784 0 ohm, C762-C765 0.1u, C766-C769 0.01u	X02-1
9	28	1/14/2008	EE	Modify HDMI detect circuit.	Added Q85,R785,R786.	X02-1
10	42	1/14/2008	EE	Change EC from ITE8512IX to ITE8512JX. The pin12 need connect to 0.1uF, 1uF.	Change R651 to C770 0.1u, pop C745 1u for EC ITE8512 rev change.	X02-1
11	12,14,	1/16/2008	EE	Follow DELL recommend to void the PCICLK5 emission issue even AMD solved it in BIOS code	Move R232 22 ohm and CLK_PCI_PCCARD signal form PCICLK5 to PCICLK1.	X02-1
P1	47	1/21/2008	P	Change to X6S material due to not support pulse charge	Change PC105, PC99, PC96 and PC108 to X6S material	X02-1
P2	51	1/21/2008	P	Derating team suggest for WCETPA	Change PR10 from 10K ohm to 11.8K ohm.	X02-1
P3	52	1/21/2008	P	Derating team suggest for WCETPA	Change PR188 from 294K ohm to 340K ohm.	X02-1
P4	54	1/21/2008	P	Derating team suggest for WCETPA	Change PR205 from 5.9K ohm to 7.5K ohm.	X02-1
				Chagne from X02-1 to X02-2		
12	28	1/29/2008	EE	DDC Capacitance over spec 50pf. We will add level shift circuit to reduce Capacitance.	Change Q1, Q2 to FDV301N. It will reduce the DDC Capacitance.	X02-2
13	15	1/29/2008	EE	Follow AMD feedback.IDE and Flash Interface Not Implemented: Decoupling caps not used.	Depop C258, C296, C298, C274, C295.	X02-2
14	15	1/29/2008	EE	Follow AMD SB700 checklist item 1-34, 1-35.	Change L35 to BLM21PG221SN1D, C330 to 10U.	X02-2
15	9, 13	1/29/2008	EE	Follow AMD RS780M item 8-7, SB700 item 7-1, 7-2 checklist to reserve PD resistor.	Reserve R787 4.7k ohm and R788, R789 10k ohm.	X02-2
16	12	1/30/2008	EE	Follow AMD SB700 checklist item 12-4 to depop RP34.	Depop RP34 8.2k ohm.	X02-2
17	9	1/30/2008	EE	Follow AMD SB700 checklist item 24-17. Change PU resistor to 300 ohm.	Change R344 4.7k to 300 ohm.	X02-2
18	13	1/30/2008	EE	Follow AMD SB700 checklist item 24-24. Depop PU resistor.	Depop R264 10k ohm.	X02-2
19	11	1/30/2008	EE	Follow AMD checklist item 17-2, 17-4, 17-6. Depop termination resistors.	Depop R343, RP22-RP32 47 ohm.	X02-2
20	9	1/30/2008	EE	Follow AMD checklist item 18-31. Depop PD resistors.	Depop R338 100k ohm.	X02-2
21	28	1/30/2008	EE	Follow EMI suggest to pop comon mode choke for HDMI.	Pop L1-L4 EXC24CG240Uand depop R6, R9, R11, R12, R14, R16, R18, R19 ohm.	X02-2
22	28	1/30/2008	EE	HDMI test Voltage level fail.	Change R317, R321, R325, R326, R330-R333 to 715 ohm.	X02-2
23	38	1/30/2008	EE	Follow EMI suggest to pop comon mode choke for USB.	Pop L19, L20 DLP11SN900HL2L. Depop R78, R83, R85, R88 0 ohm.	X02-2
24	29	1/30/2008	EE	OTP change to 85C.THERM_ALERT#_C and SYS_SHDN# leakage will affect OTP thermal limit.	Change OTP resistor to 10k, 6.8k ohm. Add D35 to prevent leakage.	X02-2
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25	27	1/31/2008	EE	Follow EMI suggest to pop caps for CRT.	Pop C455, C462, C476 22pF and C456, C464, C478, C79, C72 10pF.	X02-2
26	9,25	2/1/2008	EE	Follow CLK Gen vendor feedback to solve EA fail.	Change R146 to 43.2 ohm, R40 to 0 ohm, C50 to 49.9 ohm.	X02-2
P5	53	2/1/2008	EE	To solve transient response fail	Change PC17~PC19, PC21, PC22, PC26.	X02-2
27	27	2/1/2008	EE	Follow AMD AN_RS780G1.pdf. DAC Output Imbalance.	Change R48, R370 to 140 ohm.	X02-2
28	42	2/12/2008	EE	Use ITE8512 pin 22 detect SB_AZ_CODEC_RST# to mute speaker pop noise.	Connect SB_AZ_CODEC_RST# and U5 pin 22.	X02-2
29	5	2/12/2008	EE	Follow ANT 4.1d. CPU_TEST23_TSTUPD need PD 300 ohm.	PD R790 300 ohm for CPU_TEST23_TSTUPD.	X02-2
30	43	2/12/2008	EE	Add JP1 pin 10 to +3.3V_ALW, let +3.3V_ALW get lower drop voltage on MMB side.	Add JP1 pin 10 to +3.3V_ALW.	X02-2
P6	50,52	2/13/2008	P	Change PU2, PU5 and PU8 VCC power rail to reduce S5 power consumption.	Change PJP2.1 to +3.3V_SUS and add PR226~PR229 0 ohm.	X02-2
31	38	2/22/2008	EE	Pop ESATA re-driver for stress ESATA signals on formal build.	Pop C726~C765, U50, depop R781~R784 and change C654, C655, C768, C769 to 0.01u.	X02-2
32	31	2/22/2008	EE	Dell recommend change caps for IDT AP test on formal build.	Change C712, C713 to 6800pF.	X02-2
Chagne from X02-2 to A00-1						
1	42	3/14/2008	EE	Chagne board ID for A00.	Pop R129 and depop R128.	A00-1
P1	53	3/14/2008	P	Follow EMI suggest.	Pop PC192, PC198, PC195 0.01u and PC193, PC196, PC199 0.1u.	A00-1
2	31,32	3/14/2008	EE	Need meet WLP4.0 : 1. Add 2.2K-ohm resistors to prevent amplifier clipping.	Add R791~R794 2.2k ohm.	A00-1
				Need meet WLP4.0 : 2. Add 220PF capacitors to allow proper dynamic range measurent.	Add C771, C772 220pF and pop C726, C727 to 220pF.	A00-1
3	7~11,27,30,38,45	3/17/2008	EE	Follow Safety request. Change USB power control IC location same as FM6 location.	Swap U7, U19 and U10, U16 location. U7 and U16 are 2062AD. Swap D33 and D18, R218 and R570	A00-1
4	38	3/18/2008	EE	TI can't finish some necessary legal submission for new 2062AD. Change to old part 2062DR.	Change U7, U16 to 2062DR (AL002062005).	A00-1
5	15,49,50,51,52,55	3/18/2008	EE	Remove Power Jump for QT build.	Remove PJP1~PJP4, PJP6~PJP8, PJP10~PJP13, PJP15~PJP17 and short PJP9.	A00-1
6	38	3/18/2008	EE	Follow QSMC request to remove USB co-lay 0 ohm.	Remove R78, R83, R85, R88 0 ohm.	A00-1
7	38	3/18/2008	EE	Change the USB Power Jump to short pad fp.	Change PJP5, PJP14 fp to SHORT-10A.	A00-1
8	42	3/19/2008	EE	Follow IT8512JX glitch.doc FA report. Depop 1uF for ITE8512JX pin 12.	Depop C745 1uF.	A00-1
10	38	3/20/2008	EE	Pericom request. Add 300ohm to reduce output swing, change AC caps to 2.2nF and set EQ to GND.	Add R795 300 ohm. Chagne C95,C96,C654,C655,C766~C769 to 2.2nF and PD U50 pin1, pin10 to GND.	A00-1
11	14, 43	3/20/2008	EE	Follow Dell request. Add LED KB BK detect function.	Add R796 100k ohm , PD R797 200k ohm to J4 pin2 and connect to U30 pin G6.	A00-1
12	28	3/20/2008	EE	Change to FDV301N will pass HDMI 7-12 HDMI detect test.	Change Q80 from MM3904 to FDV301N.	A00-1
13	59	3/26/2008	EE	Follow EMI team request, add two EMI SPRING near sniffer switch area and HDMI connector.	Add PV1 near SW1 and PV2 near CN3.	A00-1
14	32	3/26/2008	EE	Follow IDT request, change 220pF to 270pF will over 80db on DTM.	Change C609, C621, C771, C772 from 220pF to 270pF.	A00-1
15	36	3/27/2008	EE	Follow EMI team request, add a 27p capacitor for 8 in 1 card reader.	Pop C760 27pF for EMI.	A00-1
P2	48	3/27/2008	EE	Follow EMI team request, add two set of 1000pF, 0.01uF, 0.1uF on J8 +DCIN_JACK , -DCIN_JACK.	Add PC200~PC202 on J8 +DCINI_JACK, PC203~PC205 on J8 -DCIN_JACK.	A00-1
P3	49, 51	3/27/2008	EE	Follow EMI team request, pop PR3, PC3 for NB_VCORE and pop PR213, PC188 for +1.8V_SUS	pop PR3, PC3 for NB_VCORE and pop PR213, PC188 for +1.8V_SUS	A00-1
16	5, 42	3/27/2008	EE	Use BID1 to control CPU_PROCHOT#. When system need change state to P1 by HTC.	Add Q86 2N7002W-F and remove R420 0 ohm for use BID1 to control CPU_PROCHOT#.	A00-1
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